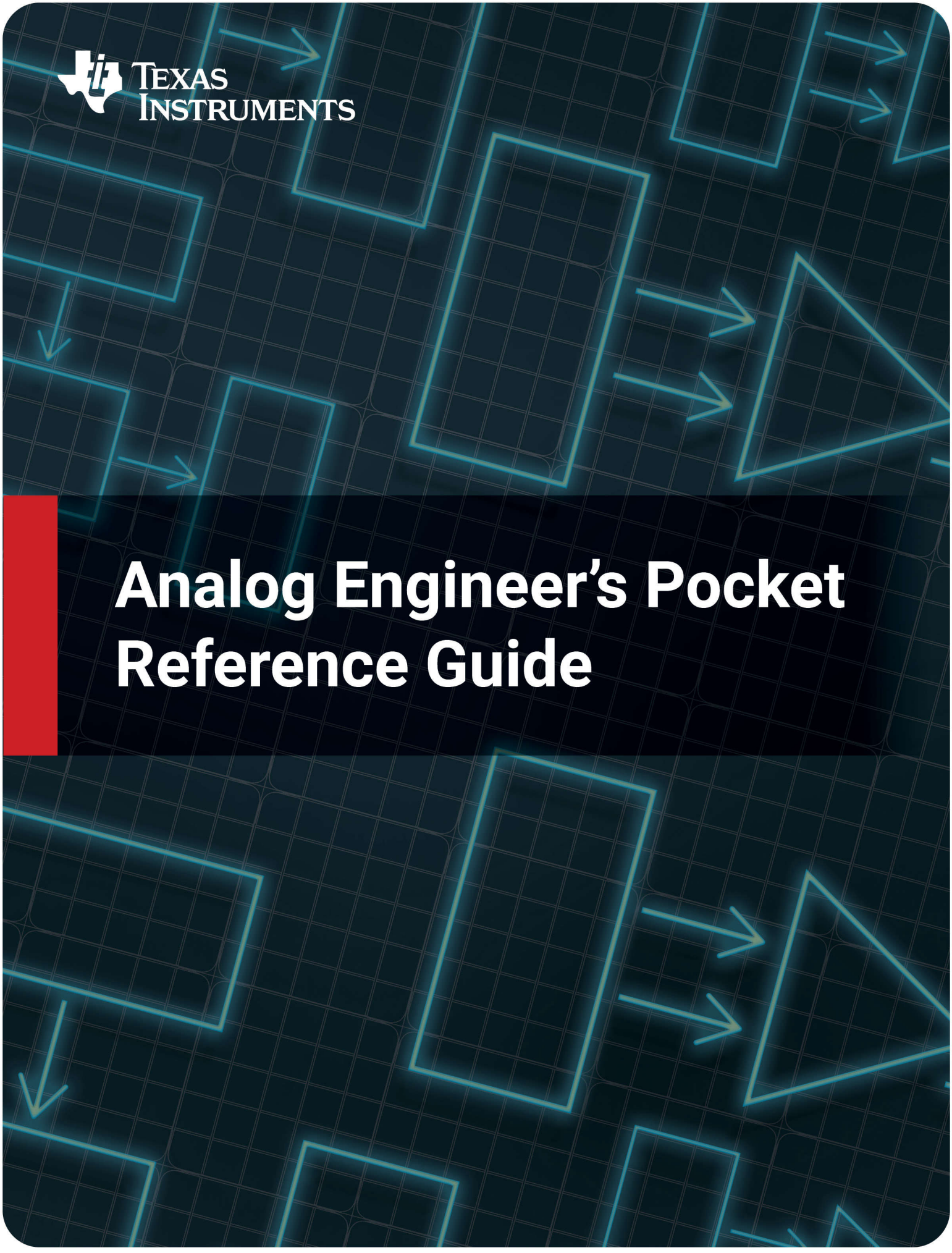
Texas Instruments
Analog Engineer's Pocket Reference Guide

Analog Engineer's Pocket Reference

Fifth Edition

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Message from the editors:

This pocket reference is intended as a valuable quick guide for often used board- and system-level design formulae. This collection of formulae is based on a combined 50 years of analog board- and system-level expertise. Much of the material herein was referred to over the years via a folder stuffed full of printouts. Those worn pages have been organized and the information is now available via this guide in a bound and hard-to-lose format!

Here is a brief overview of the key areas included:

- Key constants and conversions
- Discrete components
- AC and DC analog equations
- Op amp basic configurations
- OP amp bandwidth and stability
- Overview of sensors
- PCB trace R, L, C
- Wire L, R, C
- Binary, hex and decimal formats
- A/D and D/A conversions

We hope you find this collection of formulae as useful as we have. Please send any comments and/or ideas you have for the next edition of the *Analog Engineer's Pocket Reference* to **artkay_timgreen@list.ti.com**

Additional resources to explore:

TI Precision Labs

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Conversions

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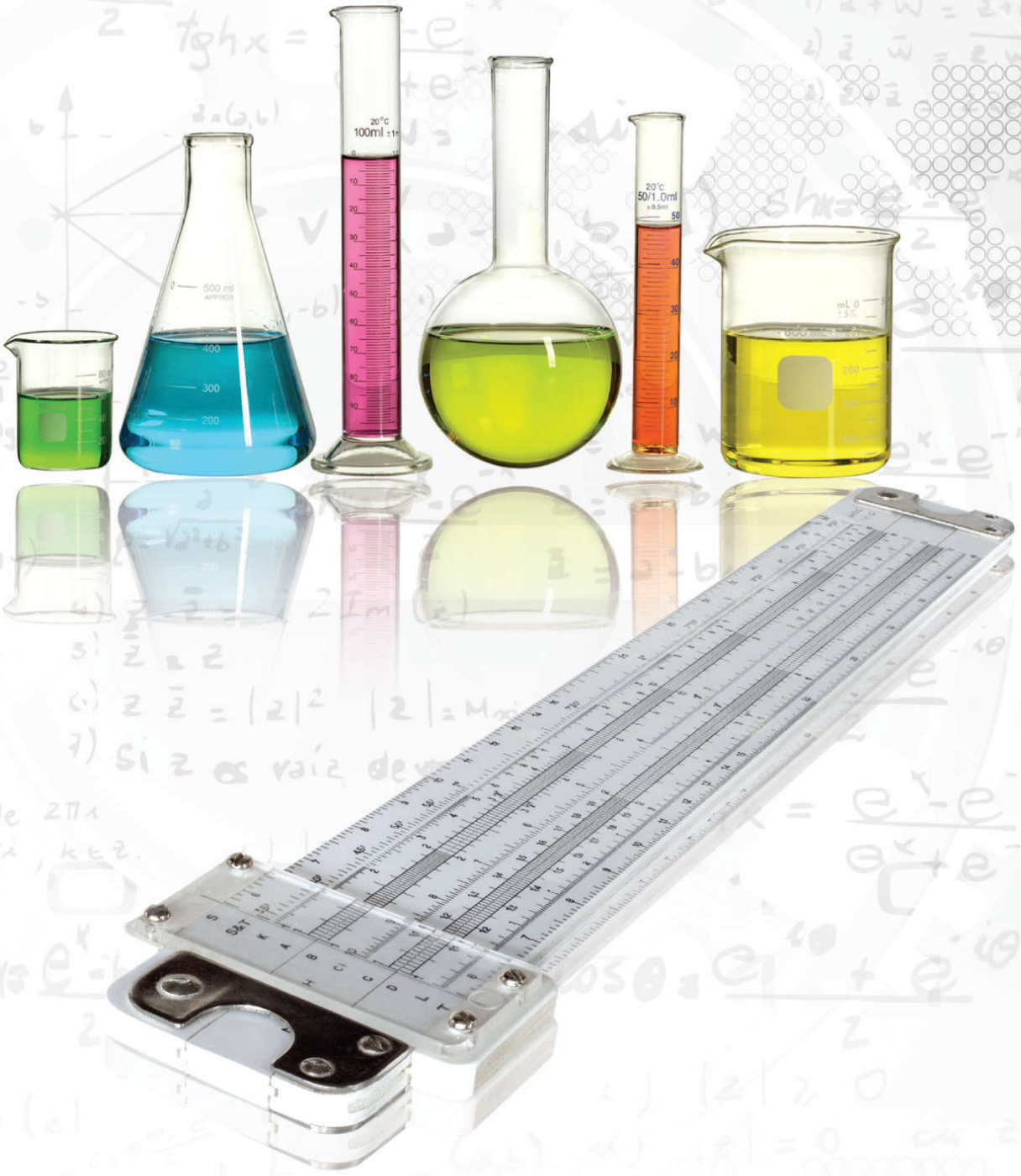


Standard decimal prefixes

Table 1. Physical constants

Constant	Symbol	Value	Units
Speed of light in a vacuum	*c*	$2.997\ 924\ 58 \times 10^{8}$	m/s
Permittivity of vacuum	e_o	$8.854187\ 817\ 620 \times 10^{-12}$	F/m
Permeability of free space	μ_o	$1.256637\ 0614 \times 10^{-6}$	H/m
Planck's constant	h	$6.626069\ 57 \times 10^{-34}$	J•s
Boltzmann's constant	k	$1.380648\ 8 \times 10^{-23}$	J/K
Faraday's constant	F	$9.648\ 533\ 99 \times 10^{4}$	C/mol
Avogadro's constant	N_A	$6.022\ 141\ 29 \times 10^{23}$	1/mol
Unified atomic massunit	m_u	$1.660538\ 921 \times 10^{-27}$	kg
Electronic charge	q	$1.602176\ 565 \times 10^{-19}$	C
Rest mass of electron	m_e	$9.109382\ 15 \times 10^{-31}$	kg
Mass of proton	m_p	$1.672621\ 777 \times 10^{-27}$	kg
Gravitational constant	G	6.67384×10^{-11}	Nm^2/kg^2
Standard gravity	g_n	9.806 65	m/s^2
Ice point	Tice	273.15	K
Maximum density of water	r	1.00×10^{3}	kg/m^3
Density of mercury (0°C)	rHg	$1.362\ 8 \times 10^{4}$	kg/m^3
Gas constant	R	8.314 462 1	J/(K•mol)
Speed of sound in air (at0°C)	*c*air	3.312×10^{2}	m/s

Table 2. Standard decimal prefixes

Multiplier	Prefix	Abbreviation
1012	tera	T
10^{9}	giga	G
10^{6}	mega	M
10^{3}	kilo	k
10–3	milli	m
10–6	micro	µ
10–9	nano	n
10–12	pico	p
10–15	femto	f
10–18	atto	a

Metric conversions

Table 3. Imperial to metric conversions

Unit	Symbol	Equivalent	Unit	Symbol
inches	in	25.4 mm/in	millimeter	mm
mil	mil	0.0254 mm/mil	millimeter	mm
feet	ft	0.3048 m/ft	meters	m
yards	yd	0.9144 m/yd	meters	m
miles	mi	1.6093 km/mi	kilometers	km
circular mil	cir mil	5.067×10^{-4} mm^2/cir mil	square millimeters	mm^2
square yards	yd^2	0.8361 m^2	square meters	$_{m}^{2}$
pints	pt	0.5682 L/pt	liters	L
ounces	oz	28.35 g/oz	grams	g
pounds	lb	0.4536 kg/lb	kilograms	kg
calories	cal	4.184 J/cal	joules	J
horsepower	hp	745.7 W/hp	watts	W

Table 4. Metric to imperial conversions

Unit	Symbol	Conversion	Unit	Symbol
millimeter	mm	0.0394 in/mm	inch	in
millimeter	mm	39.4 mil/mm	mil	mil
meters	m	3.2808 ft/m	feet	ft
meters	m	1.0936 yd/m	yard	yd
kilometers	km	0.6214 mi/km	miles	mi
square millimeters	mm^2	1974 cir mil/mm^2	circular mil	cir mil
square meters	$_{m}^{2}$	1.1960 yd^2/m^2	square yards	yd^2
liters	L	1.7600 pt/L	pints	pt
grams	g	0.0353 oz/g	ounces	oz
kilograms	kg	2.2046 lb/kg	pounds	lb
joules	J	0.239 cal/J	calories	cal
watts	W	1.341×10^{-3} hp/W	horsepower	hp

Example

Convert 10 mm to mil.

Answer

$$10\ \text{mm} \times 39.4 \frac{\text{mil}}{\text{mm}} = 394\ \text{mil} \quad (1)$$

Temperature scale conversions

Table 5. Temperature conversions

$°C = \frac{5}{9}(°F - 32)$	Fahrenheit to Celsius
$°F = \frac{9}{5}(°C) + 32$	Celsius to Fahrenheit
$K = °C + 273.15$	Celsius to Kelvin
$°C = K - 273.15$	Kelvin to Celsius

Table 6. Error conversions

$\text{Error}(\%) = \frac{\text{Measured}-\text{Ideal}}{\text{Ideal}} \times 100$	Error in measured value
$\text{Error}(\%\text{FSR}) = \frac{\text{Measured-Ideal}}{\text{Full-scale range}} \times 100$	Error in percent of full-scale range
$\% = \frac{\text{ppm}}{10^6} \times 100$	Part per million to percent
$\text{m}\% = \frac{\text{ppm}}{10^6} \times 100 \times 1000$	Part per million to milli-percent
ppm = % × 10^4	Percent to part per million
ppm = m% × 10	Milli-percent to part per million

Example

Compute the error for a measured value of 0.12V when the ideal value is 0.1V and the range is 5V.

Answer

$$\text{Error}(\%) = \frac{0.12\text{V} - 0.1\text{V}}{0.1\text{V}} \times 100 = 20\% \quad \text{Error in measured value}$$
$$\text{Error}(\%\ \text{FSR}) = \frac{0.12 - 0.1\text{V}}{5\text{V}} \times 100 = 0.4\% \quad \text{Percent FSR} \tag{2}$$

Example

Convert 10 ppm to percent and milli-percent.

Answer

$$\frac{10\ \text{ppm}}{10^6} \times 100 = 0.001\% \quad \text{Part per million to percent}$$
$$\frac{10\ \text{ppm}}{10^6} \times 100 \times 1000 = 1\ \text{m}\% \quad \text{Part per million to milli-percent} \tag{3}$$

Error conversions ppm and percentage

Table 7. Conversion between codes, mV, %, and ppm

	Codes	mV	%	ppm
Codes	*	$\text{Codes} \cdot \left(\frac{V_{FSR}}{2^N}\right) \cdot 1000$	$\text{Codes} \cdot \left(\frac{1}{2^N}\right) \cdot 100$	$\text{Codes} \cdot \left(\frac{1}{2^N}\right) \cdot 10^6$
mV	$\text{mV} \cdot \left(\frac{2^N}{V_{FSR} \cdot 1000}\right)$	*	$\text{mV} \cdot \left(\frac{1}{V_{FSR} \cdot 1000}\right) \cdot 100$	$\text{mV} \cdot \left(\frac{1}{V_{FSR} \cdot 1000}\right) \cdot 10^6$
%	$\% \cdot \left(\frac{2^N}{100}\right)$	$\% \cdot \left(\frac{V_{FSR} \cdot 1000}{100}\right)$	*	$\% \cdot \left(\frac{10^6}{100}\right)$
ppm	$\text{ppm} \cdot \left(\frac{2^N}{10^6}\right)$	$\text{ppm} \cdot \left(\frac{V_{FSR} \cdot 1000}{10^6}\right)$	$\text{ppm} \cdot \left(\frac{1}{10^6}\right) \cdot 100$	*

Where

N = resolution of ADC

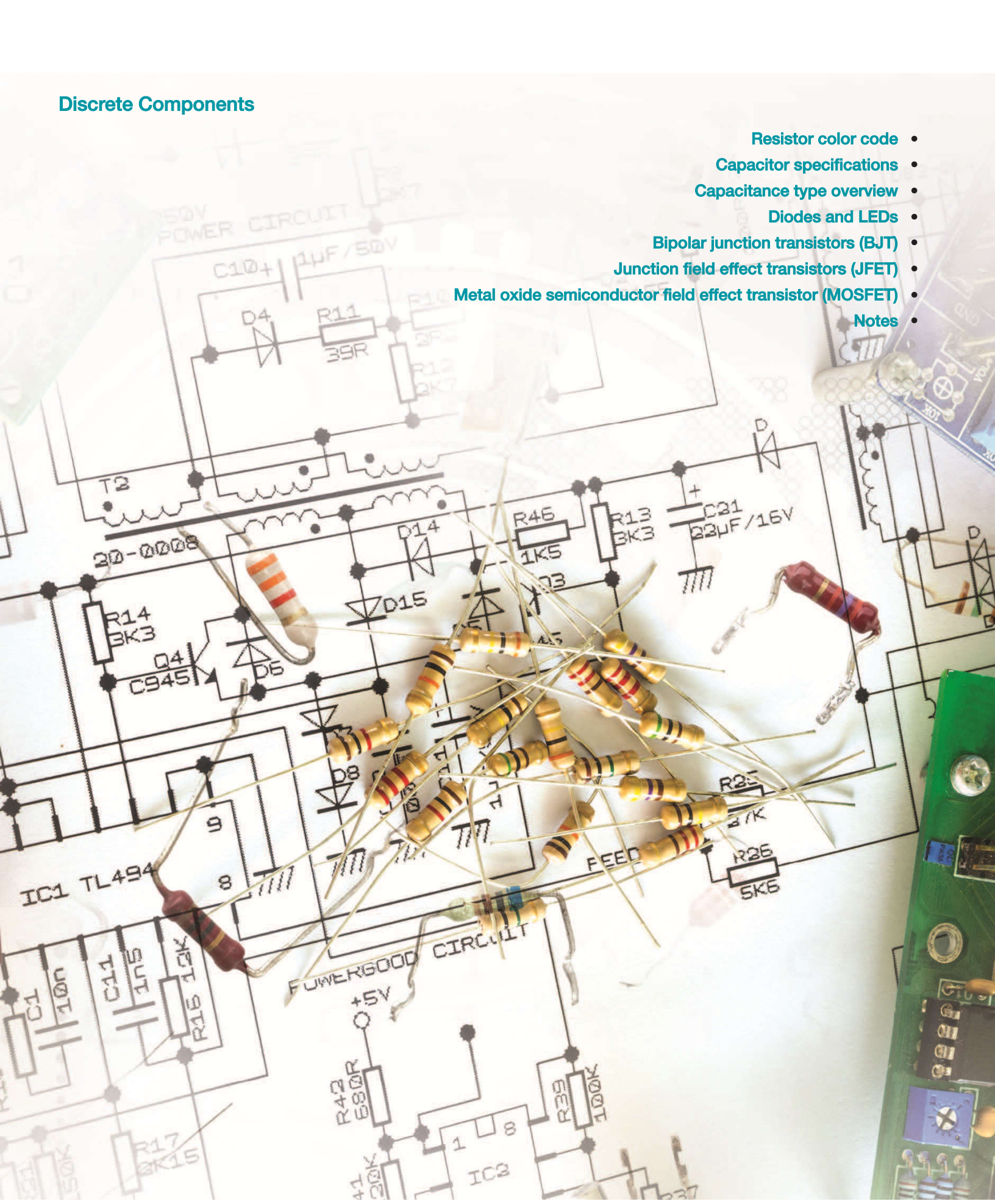
V_{FSR} = full scale range of ADC in voltage. Full scale range is double for a bipolar ADC compared with unipolar ADC.

Codes, %, and ppm = the equivalent value ADC codes, percentage, and parts per million

Notes

Discrete Components

- Resistor color code
- Capacitor specifications
- Capacitance type overview
- Diodes and LEDs
- Bipolar junction transistors (BJT)
- Junction field effect transistors (JFET)
- Metal oxide semiconductor field effect transistor (MOSFET)
- Notes



Resistor color code

Table 8. Resistor color code

Color	Digit	Additional Zeros	Tolerance	Temperature Coefficient	Failure Rate
Black	0	0		250	
Brown	1	1	1%	100	1
Red	2	2	2%	50	0.1
Orange	3	3		15	0.01
Yellow	4	4		25	0.001
Green	5	5	0.5%	20	
Blue	6	6	0.25%	10	
Violet	7	7	0.1%	5	
Grey	8	8	0.05%	1	
White	9	9			
Gold	-na-	–1	5%		
Silver	-na-	–2	10%		
No Band	-na-	-na-	20%		

4 band example: yellow violet orange silver indicate 4,7 and 3 zeros;

i.e. a 47kΩ, 10% resistor.

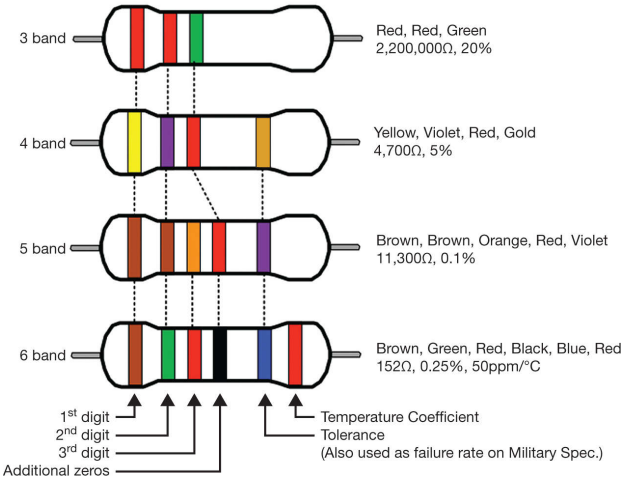


Figure 1. *Resistor color code examples*

Table 9. Standard resistor values

Standard resistance values for the 10 to 100 decade																	
0.1% 0.25% 0.5%	1%	2% 5% 10%	0.1% 0.25% 0.5%	1%	2% 5% 10%	0.1% 0.25% 0.5%	1%	2% 5% 10%	0.1% 0.25% 0.5%	1%	2% 5% 10%	0.1% 0.25% 0.5%	1%	2% 5% 10%	0.1% 0.25% 0.5%	1%	2% 5% 10%
10.0	10.0	10	14.7	14.7		21.5	21.5		31.6	31.6		46.4	46.4		68.1	68.1	68
10.1			14.9			21.8			32.0			47.0		47	69.0		
10.2	10.2		15.0	15.0	15	22.1	22.1	22	32.4	32.4		47.5	47.5		69.8	69.8	
10.4			15.2			22.3			32.8			48.1			70.6		
10.5	10.5		15.4	15.4		22.6	22.6		33.2	33.2	33	48.7	48.7		71.5	71.5	
10.6			15.6			22.9			33.6			49.3			72.3		
10.7	10.7		15.8	15.8		23.2	23.2		34.0	34.0		49.9	49.9		73.2	73.2	
10.9			16.0		16	23.4			34.4			50.5			74.1		
11.0	11.0	11	16.2	16.2		23.7	23.7		34.8	34.8		51.1	51.1	51	75.0	75.0	75
11.1			16.4			24.0		24	35.2			51.7			75.9		
11.3	11.3		16.5	16.5		24.3	24.3		35.7	35.7		52.3	52.3		76.8	76.8	
11.4			16.7			24.6			36.1		36	53.0			77.7		
11.5	11.5		16.9	16.9		24.9	24.9		36.5	36.5		53.6	53.6		78.7	78.7	
11.7			17.2			25.2			37.0			54.2			79.6		
11.8	11.8		17.4	17.4		25.5	25.5		37.4	37.4		54.9	54.9		80.6	80.6	
12.0		12	17.6			25.8			37.9			55.6			81.6		
12.1	12.1		17.8	17.8		26.1	26.1		38.3	38.3		56.2	56.2	56	82.5	82.5	82
12.3			18.0		18	26.4			38.8			56.9			83.5		
12.4	12.4		18.2	18.2		26.7	26.7		39.2	39.2	39	57.6	57.6		84.5	84.5	
12.6			18.4			27.1		27	39.7			58.3			85.6		
12.7	12.7		18.7	18.7		27.4	27.4		40.2	40.2		59.0	59.0		86.6	86.6	
12.9			18.9			27.7			40.7			59.7			87.6		
13.0	13.0	13	19.1	19.1		28.0	28.0		41.2	41.2		60.4	60.4		88.7	88.7	
13.2			19.3			28.4			41.7			61.2			89.8		
13.3	13.3		19.6	19.6		28.7	28.7		42.2	42.2		61.9	61.9	62	90.9	90.9	91
13.5			19.8			29.1			42.7			62.6			92.0		
13.7	13.7		20.0	20.0	20	29.4	29.4		43.2	43.2	43	63.4	63.4		93.1	93.1	
13.8			20.3			29.8			43.7			64.2			94.2		
14.0	14.0		20.5	20.5		30.1	30.1	30	44.2	44.2		64.9	64.9		95.3	95.3	
14.2			20.8			30.5			44.8			65.7			96.5		
14.3	14.3		21.0	21.0		30.9	30.9		45.3	45.3		66.5	66.5		97.6	97.6	
14.5			21.3			31.2			45.9			67.3			98.8		

Capacitor specifications

Practical capacitor model and specifications

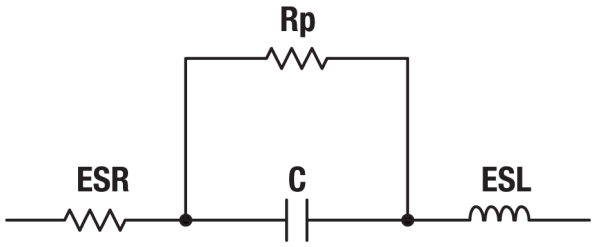


Figure 2. *Model of a practical capacitor*

Table 10. Capacitor specifications

Parameter	Description
C	The nominal value of the capacitance **Table 12** lists standard capacitance values
ESR	Equivalent series resistance Ideally this is zero Ceramic capacitors have the best ESR (typically in milliohms). Tantalum Electrolytic have ESR in the hundreds of milliohms and Aluminum Electrolytic have ESR in the ohms
ESL	Equivalent series inductance Ideally this is zero ESL ranges from 100 pH to 10 nH
Rp	Rp is a parallel leakage resistance (or insulation resistance) Ideally this is infinite This can range from tens of megaohms for some electrolytic capacitors to tens of gigohms for ceramic
Voltage rating	The maximum voltage that can be applied to the capacitor Exceeding this rating damages the capacitor
Voltage coefficient	The change in capacitance with applied voltage in ppm/V A high-voltage coefficient can introduce distortion C0G capacitors have the lowest coefficient The voltage coefficient is most important in applications that use capacitors in signal processing such as filtering
Temperature coefficient	The change in capacitance with across temperature in ppm/°C Ideally, the temperature coefficient is zero The maximum specified drift generally ranges from 10 to 100ppm/°C or greater depending on the capacitor type (See **Table 11** for details)

Capacitance type overview

Practical capacitors vs. frequency

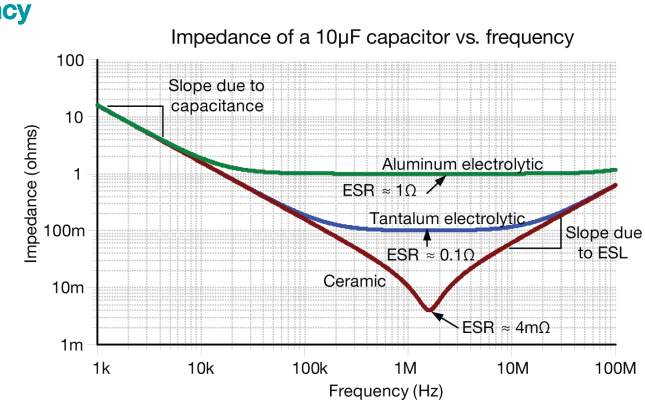


Figure 3. *Effect of ESR and ESL on capacitor frequency response*

Table 11. Capacitor type overview

Capacitor type	Description
C0G/NP0 **(Type 1 ceramic)**	Use in signal path, filtering, low distortion, audio, and precision Limited capacitance range: 0.1 pF to 0.47 µF Lowest temperature coefficient: ±30 ppm/°C Low-voltage coefficient Minimal piezoelectric effect Good tolerance: ±1% to ±10% Temperature range: –55°C to 125°C (150°C and higher) Voltage range may be limited for larger capacitance values
X7R **(Type 2 ceramic)**	Use for decoupling and other applications where accuracy and low distortion are not required X7R is an example of a type 2 ceramic capacitor See EIA capacitor tolerance table for details on other types Capacitance range: 10 pF to 47 µF Temperature coefficient: ±833 ppm/°C (±15% across temp range) Substantial voltage coefficient Tolerance: ±5% to –20%/+80% Temperature range: –55°C to 125°C Voltage range may be limited for larger capacitance values
Y5V **(Type 2 ceramic)**	Use for decoupling and other applications where accuracy and low distortion are not required Y5V is an example of a type 2 ceramic capacitor See EIA capacitor tolerance table for details on other types Temperature coefficient: –20%/+80% across temp range Temperature range: –30°C to 85°C Other characteristics are similar to X7R and other type 2 ceramic

Table 11. Capacitor type overview (continued)

Capacitor type	Description
Aluminum oxide electrolytic	Use for bulk decoupling and other applications where large capacitance is required Note that electrolytic capacitors are polarized and will be damaged, if a reverse polarity connection is made Capacitance range: 1 µF to 68,000 µF Temperature coefficient: ±30 ppm/°C Substantial voltage coefficient Tolerance: ±20% Temperature range: –55°C to 125°C (150°C and higher) Higher ESR than other types
Tantalum electrolytic	Capacitance range: 1 µF to 150 µF Similar to aluminum oxide but smaller size
Polypropylene film	Capacitance range: 100 pF to 10 µF Very low voltage coefficient (low distortion) Higher cost than other types Larger size per capacitance than other types Temperature coefficient: 2% across temp range Temperature range: –55°C to 100°C

Table 12. Standard capacitance

Standard capacitance table											
1	1.1	1.2	1.3	1.5	1.6	1.8	2	2.2	2.4	2.7	3
3.3	3.6	3.9	4.3	4.7	5.1	5.6	6.2	6.8	7.5	8.2	9.1

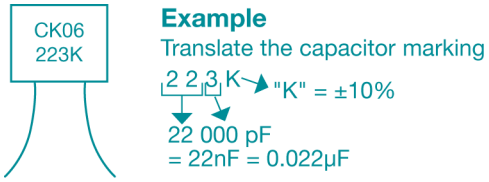


Figure 4. *Capacitor marking code*

Table 13. Ceramic capacitor tolerance markings

Code	Tolerance	Code	Tolerance
B	± 0.1 pF	J	± 5%
C	± 0.25 pF	K	± 10%
D	± 0.5 pF	M	± 20%
F	± 1%	Z	+ 80%, –20%
G	± 2%		

Table 14. EIA capacitor tolerance markings (Type 2 capacitors)

First letter symbol	Low temp limit	Second number symbol	High temp limit	Second letter symbol	Max. capacitance change over temperature rating
Z	+10°C	2	+45°C	A	±1.0%
Y	–30°C	4	+65°C	B	±1.5%
X	–55°C	5	+85°C	C	±2.2%
		6	+105°C	D	±3.3%
		7	+125°C	E	±4.7%
				F	±7.5%
				P	±10.0%
				R	±15.0%
				S	±22.0%
				T	±22% ~ 33%
				U	±22% ~ 56%
				V	±22% ~ 82%

Example

X7R: –55°C to +125°C, ±15.0%

Diodes and LEDs

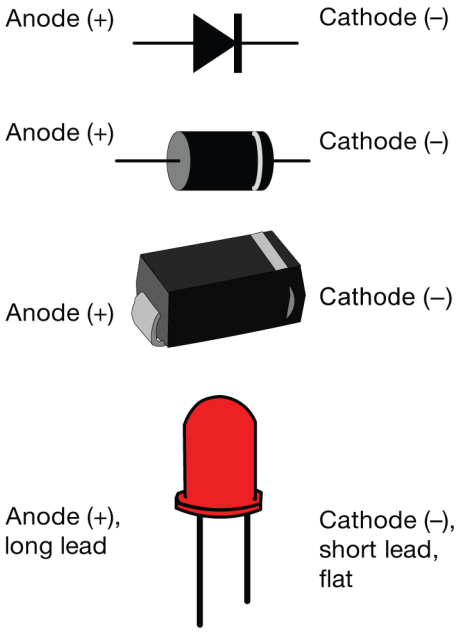


Figure 5. *Diode and LED pin names*

Table 15. LED forward voltage drop by color

Color	Wavelength (nm)	Voltage (approximate range)
Infrared	940-850	1.4 to 1.7
Red	660-620	1.7 to 1.9
Orange / Yellow	620-605	2 to 2.2
Green	570-525	2.1 to 3.0
Blue/White	470-430	3.4 to 3.8

Note

The voltages given are approximate, and are intended to show the general trend for forward voltage drop of LED diodes. Consult the manufacturer's data sheet for more precise values.

Bipolar junction transistors (BJT)

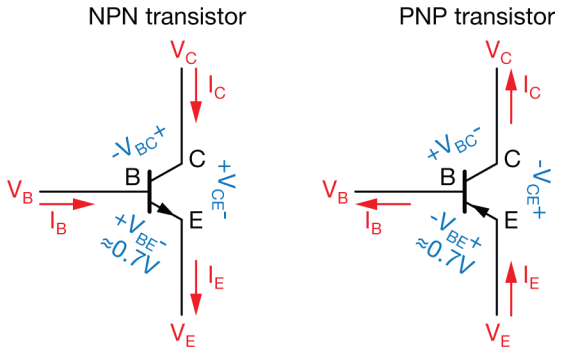


Figure 6. *Bipoloar transistors*

Current gain

$$I_C = I_B \cdot \beta \tag{4}$$

Current law for bipolar transistors

$$I_C = I_B + I_E \tag{5}$$

Voltage base to emitter is forward bias for normal operation. Approximately 0.7V.

$$V_{BE} \approx 0.7V \tag{6}$$

Voltage base to collector is reverse bias for normal operation

$$V_{BC} \text{ is reversed biased} \tag{7}$$

Collector to emitter voltage

$$V_{CE} \approx V_{BC} + V_{BE} \tag{8}$$

Where

B, E, C = base, emitter, and collector

I_B, I_E, I_C = base, emitter, and collector current

$\beta = h_{fe}$ = current gain

V_{CE}= collector to emitter voltage

V_{BC} = base to collector voltage

V_{BE} = base to emitter voltage

Junction field effect transistors (JFET)

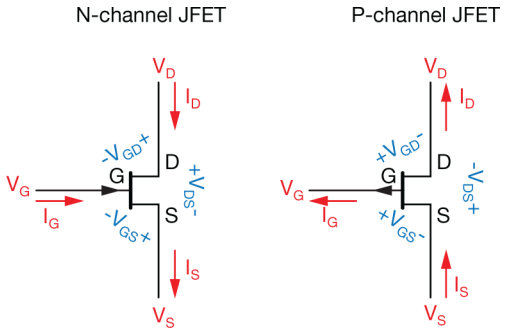


Figure 7. *JFET transistors*

Gate to source reverse biased for normal operation

$$I_G \approx 0V \tag{9}$$

Drain current equal to source current

$$I_D = I_S \tag{10}$$

Drain current in linear region

$$I_D = \frac{2I_{DSS}}{V_P{}^2}\left(V_{GS} - V_P - \frac{V_{DS}}{2}\right)V_{DS} \tag{11}$$

Drain current in saturation region

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{12}$$

Where

G, D, S = gate, drain, and source

I_{DSS} = saturation current at zero gate to source voltage

V_P = pinch off voltage where the drain-to-source current stops

$I_D = I_S$ = drain current, source current. These will be equal.

V_{GS} = gate to source voltage

V_{DS} = drain to source voltage

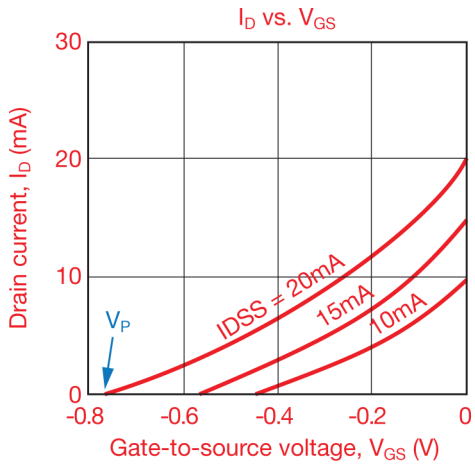


Figure 8. *N-channel JFET characteristic curve I_D vs V_{GS}*

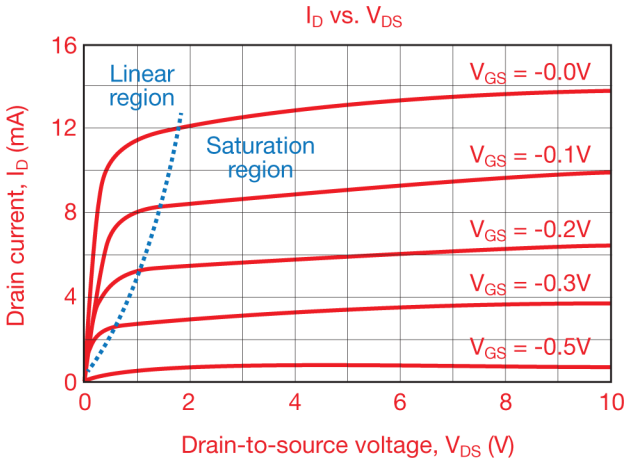


Figure 9. *N-channel JFET characteristic curve I_D vs V_{GS}*

- The maximum gate-to-source voltage is 0V for an N-channel JFET. Greater than 0V will forward bias the gate-to-source junction and cause abnormal operation.
- The P-channel FET has similar characteristic curves but the polarity is opposite.

Metal oxide semiconductor field effect transistor (MOSFET)

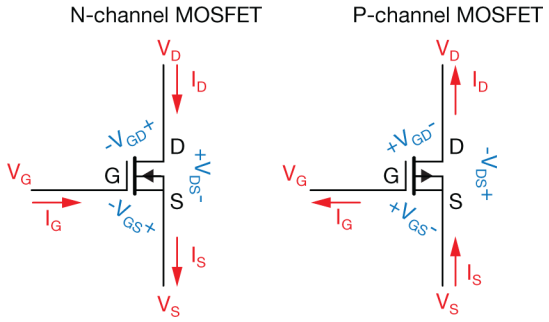


Figure 10. *MOSFET transistors*

Gate is insulated so that input current is negligible

$$I_G \approx 0A \tag{13}$$

Drain current equal to source current

$$I_D = I_S \tag{14}$$

Drain current in linear region (triode)

$$I_D = \mu_n C_{OX} \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{15}$$

Drain current in saturation region

$$I_D = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda(V_{DS} - V_{DSsat})) \tag{16}$$

Where

G, D, S = gate, drain, and source

μ_n = charge-carrier effective mobility

C_{OX} = capacitance of oxide

W, L = width and length of gate

V_{GS} = gate to source voltage

V_{DS} = drain to source voltage

V_{TH} = threshold voltage

λ = channel length modulation

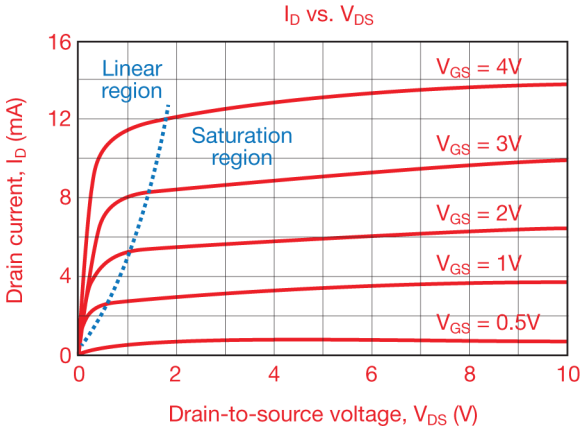


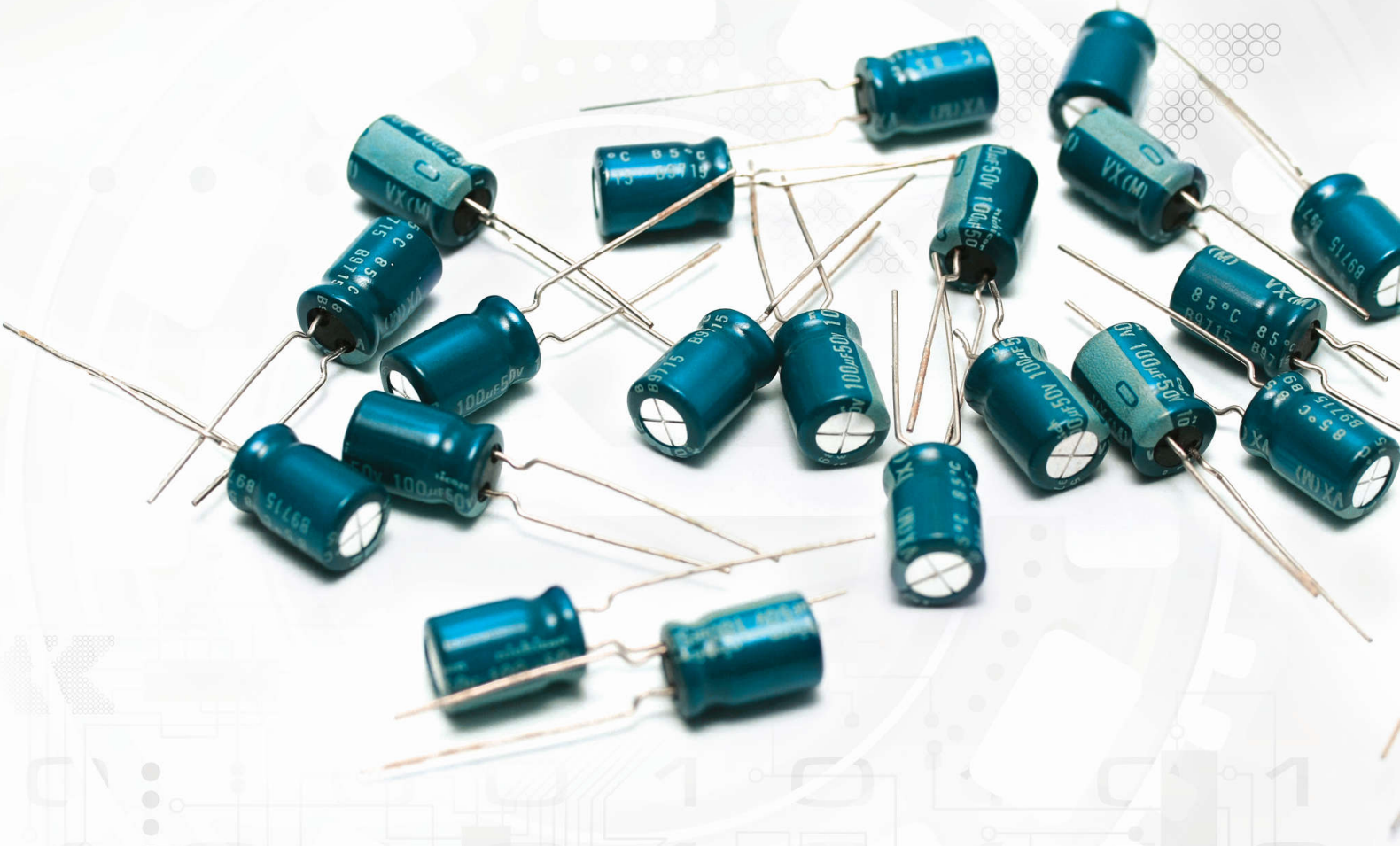
Figure 11. *N-channel MOSFET characteristic curve, I_D vs. V_{DS}*

- The parameters, such as μ_n, C_{OX}, W, and L, may not be given in discrete MOSFET data sheets.
- The P-channel FET has similar characteristic curves but the polarity is opposite.

Notes

Analog

- Resistor equations
- Power equations
- Capacitor equations
- Inductor equations
- RMS and mean voltage
- Logarithmic mathematical definitions
- dB definitions
- Pole (equations)
- Notes



Resistor equations

Series resistors

$$R_T = R_1 + R_2 + \cdots + R_N \tag{17}$$

Two parallel resistors

$$R_T = \frac{R_1 \cdot R_2}{R_1 + R_2} \tag{18}$$

Parallel resistors

$$R_T = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_N}} \tag{19}$$

Where

R_T = equivalent total resistance

R_1, R_2, R_3, …R_N = component resistors

Ohm's law and voltage divider equation

Ohm's law

$$V = I \cdot R \tag{20}$$

Voltage divider equation

$$V_{OUT} = \left(\frac{R_2}{R_1 + R_2}\right) \cdot V_{sup} \tag{21}$$

Where

V = voltage in volts (V)

I = current in amps (A)

R = resistance in ohms (Ω)

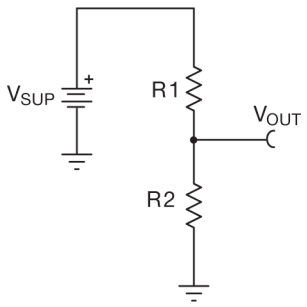


Figure 12. *Voltage divider*

Power equations

Power equation for voltage and current

$$P = I \cdot V \tag{22}$$

Power equation for voltage and resistance

$$P = \frac{V^2}{R} \tag{23}$$

Power equation for current and resistance

$$P = I^2 \cdot R \tag{24}$$

Where

P = power in watts (W)

V = voltage in volts (V)

I = current in amps (A)

R = resistance in ohms (Ω)

AC power equation

$$P = \frac{1}{2} \cdot V_P \cdot I_P \cdot \cos\theta \tag{25}$$

Where

P = average power in watts (W) for sinusoidal signals

V_p = peak voltage in volts (V)

I_p = peak current in amps (A)

θ = phase angle between the voltage and current sine waves

Capacitor equations

Series capacitors

$$C_t = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \ldots + \frac{1}{C_N}} \tag{26}$$

Two series capacitors

$$C_t = \frac{C_1 C_2}{C_1 + C_2} \tag{27}$$

Parallel capacitors

$$C_t = C_1 + C_2 + ... + C_N \quad (28)$$

Where

C_t = equivalent total capacitance

C_1, C_2, C_3…C_N = component capacitors

Charge storage

$$Q=CV \quad (29)$$

Charge defined

$$Q=It \quad (30)$$

Where

Q = charge in coulombs (C)

C = capacitance in farads (F)

V = voltage in volts (V)

I = current in amps (A)

t = time in seconds (s)

Instantaneous current through a capacitor

$$i = C\frac{dv}{dt} \quad (31)$$

Where

i = instantaneous current through the capacitor

C = capacitance in farads (F)

$\frac{dv}{dt}$ = the instantaneous rate of voltage change dt

Energy stored in a capacitor

$$E = \frac{1}{2}CV^2 \quad (32)$$

Where

E = energy stored in a capacitor in joules (J)

V = voltage in volts

C = capacitance in farads (F)

Inductor equations

Series inductors

$$L_t = L_1 + L_2 + ... + L_N \quad (33)$$

Parallel inductors

$$L_t = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + ... + \frac{1}{L_N}} \quad (34)$$

Two parallel inductors

$$L_t = \frac{L_1 L_2}{L_1 + L_2} \quad (35)$$

Where

L_t = equivalent total inductance

L_1, L_2, L_3…L_N = component inductance

Instantaneous voltage across an inductor

$$v = L\frac{di}{dt} \quad (36)$$

Where

v = instantaneous voltage across the inductor

L = inductance in henries (H)

$\frac{di}{dt}$ = instantaneous rate of current change

Energy stored in an inductor

$$E = \frac{1}{2} L I^2 \quad (37)$$

Where

E = energy stored in an inductor in joules (J)

I = current in amps

L = inductance in henries (H)

Equation for charging an RC circuit

General relationship

$$V_C = V_S\left[1 - e^{\left(\frac{-t}{\tau}\right)}\right] \tag{38}$$

Where

V_C = voltage across the capacitor at any instant in time (t)

V_S = the source voltage charging the RC circuit

t = time in seconds

τ = RC, the time constant for charging and discharging capacitors

Graphing **Equation 37** produces the capacitor charging curve below. Note that the capacitor is 99.3% charged at five time constants. It is common practice to consider this *fully charged.*

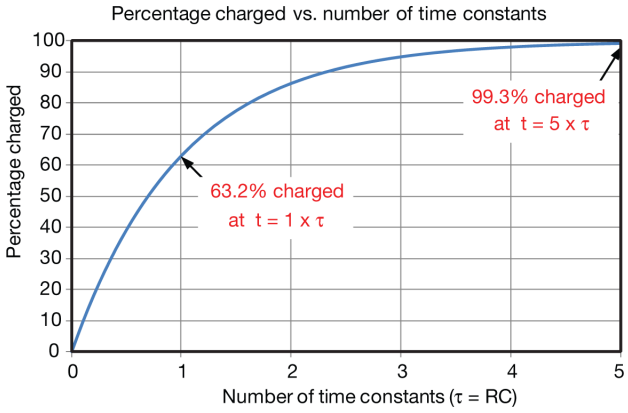


Figure 13. *RC charge curve*

General Relationship

$$V_C = V_i\left[e^{\left(\frac{-t}{\tau}\right)}\right] \tag{39}$$

Where

V_C = voltage across the capacitor at any instant in time (t)

V_i = the initial voltage of the capacitor at t = 0s

t = time in seconds

τ = RC, the time constant for charging and discharging capacitors

Graphing **Equation 39** produces the capacitor discharge curve below. Note that the capacitor is discharged to 0.7% at five time constants. It is common practice to consider this *fully discharged.*

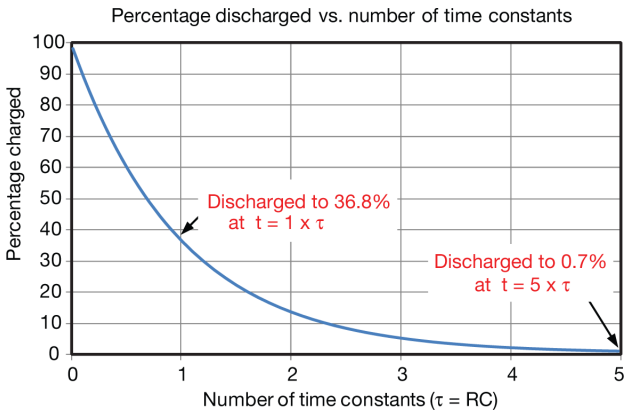


Figure 14. *RC discharge curve*

Capacitor with constant current source

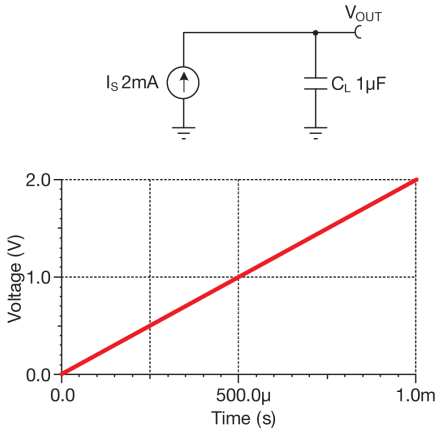


Figure 15. *Capacitor with constant current source*

General equation for capacitor voltage current

$$dv = \frac{i}{C}dt \tag{40}$$

For constant current

$$V_{OUT} = \frac{I_S}{C_L}t \tag{41}$$

Where

I_S = constant current source in amps (A)

V_{OUT} = voltage developed across the capacitor in volts (V)

C_L = load capacitance in farads (F)

t = time in seconds (s)

RMS and mean voltage

RMS voltage

General relationship

$$V_{RMS} = \sqrt{\frac{1}{(T_2 - T_1)} \int_{T1}^{T2} [V(t)]^2 dt} \quad (42)$$

Where

V(t) = continuous function of time

t = time in seconds

$T_1 \leq t \leq T_2$ = the time interval that the function is defined over

Mean voltage

General relationship

$$V_{MEAN} = \frac{1}{(T_2 - T_1)} \int_{T1}^{T2} V(t) dt \quad (43)$$

Where

V(t) = continuous function of time

t = time in seconds

$T_1 \leq t \leq T_2$ = the time interval that the function is defined over

RMS for full wave rectified sine wave

$$V_{RMS} = \frac{V_{PEAK}}{\sqrt{2}} \quad (44)$$

Mean for full wave rectified sine wave

$$V_{MEAN} = \frac{2 \times V_{PEAK}}{\pi} \quad (45)$$

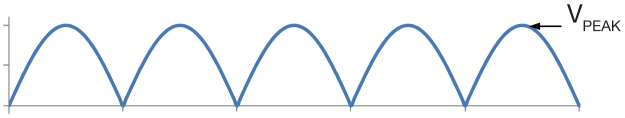


Figure 16. *Full wave rectified sine wave*

RMS for a half-wave rectified sine wave

$$V_{RMS} = V_{PEAK} \sqrt{\frac{\tau}{2T}} \quad (46)$$

Mean for a half-wave rectified sine wave

$$V_{MEAN} = \frac{2 \cdot V_{PEAK}}{\pi}\left(\frac{\tau}{T}\right) \quad (47)$$

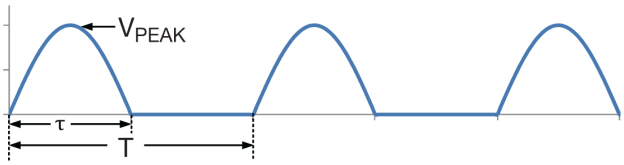


Figure 17. *Half-wave rectified sine wave*

RMS for a square wave

$$V_{RMS} = V_{PEAK}\sqrt{\frac{\tau}{T}} \quad (48)$$

Mean for a square wave

$$V_{MEAN} = V_{PEAK}\left(\frac{\tau}{T}\right) \quad (49)$$

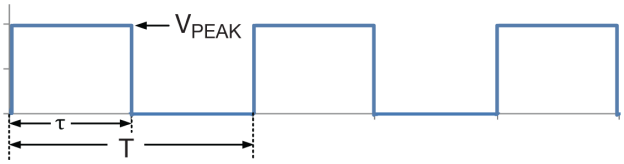


Figure 18. *Square wave*

RMS for a trapezoid

$$V_{RMS} = \sqrt{\left(\frac{V_a{}^2 + V_a \cdot V_b + V_b{}^2}{3}\right)\left(\frac{\tau}{T}\right)} \quad (50)$$

Mean for a trapezoid

$$V_{MEAN} = \frac{\tau}{2T}(V_a + V_b) \quad (51)$$

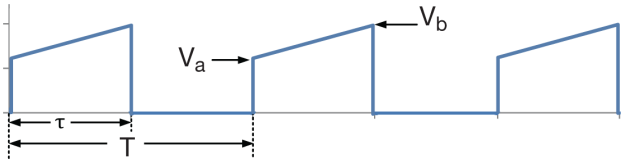


Figure 19. *Trapezoidal wave*

RMS for a triangle wave

$$V_{RMS} = V_{PEAK}\sqrt{\frac{\tau}{3T}} \quad (52)$$

Mean for a triangle wave

$$V_{MEAN} = \frac{\tau}{2T} \quad V_{PEAK} \quad (53)$$

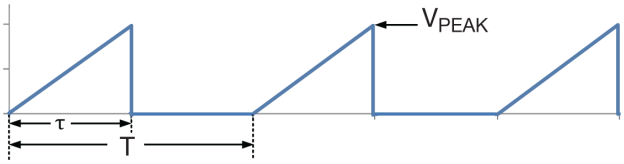


Figure 20. *Triangle wave*

Logarithmic mathematical definitions

Log of dividend

$$\log\left(\frac{A}{B}\right) = \log(A) - \log(B) \tag{54}$$

Log of product

$$\log(AB) = \log(A) + \log(B) \tag{55}$$

Log of exponent

$$\log\left(A^{x}\right) = x\log(A) \tag{56}$$

Changing the base of log function

$$\log_b(X) = \frac{\log_a(X)}{\log_a(b)} \tag{57}$$

Example changing to log base 2

$$\log_2(X) = \frac{\log_{10}(X)}{\log_{10}(2)} \tag{58}$$

Natural log is log base e

$$\ln(X) = \log_e(X) \tag{59}$$

Exponential function to 6 digits

$$e = 2.718282 \tag{60}$$

Alternative notations

$$\exp(x) = e^{x} \tag{61}$$

Figure 21. *Different notation for exponential function*

$$3.54E-2 = 3.54 \times 10^{-2} \tag{62}$$

Figure 22. *Different notation for scientific notation, sometimes confused with exponential function*

dB definitions

Bode plot basics

The frequency response for the magnitude or gain plot is the change in voltage gain as frequency changes. This change is specified on a Bode plot, a plot of frequency versus voltage gain in dB (decibels). Bode plots are usually plotted as semi-log plots with frequency on the x-axis, log scale, and gain on the y-axis, linear scale. The other half of the frequency response is the phase shift versus frequency and is plotted as frequency versus degrees phase shift. Phase plots are usually plotted as semi-log plots with frequency on the x-axis, log scale, and phase shift on the y-axis, linear scale.

Definitions

Voltage gain in decibels

$$\text{Voltage gain (dB)} = 20\log\left(\frac{V_{OUT}}{V_{IN}}\right) \tag{63}$$

Power gain in decibels

$$\text{Power gain (dB)} = 10\log\left(\frac{P_{OUT}}{P_{IN}}\right) \tag{64}$$

Used for input or output power

$$\text{Power measured (dBm)} = 10\log\left(\frac{\text{Power measured (W)}}{1\text{ mW}}\right) \tag{65}$$

Table 16. Examples of common gain values and dB equivalent

A (V/V)	A (dB)
0.001	–60
0.01	–40
0.1	–20
1	0
10	20
100	40
1,000	60
10,000	80
100,000	100
1,000,000	120
10,000,000	140

Roll-off rate is the decrease in gain with frequency

Decade is a tenfold increase or decrease in frequency (from 10 Hz to 100 Hz is one decade)

Octave is the doubling or halving of frequency (from 10 Hz to 20 Hz is one octave)

Log scale

Figure 23 illustrates a method to graphically determine values on a logarithmic axis that are not directly on an axis grid line.

1. Given L = 1cm; D = 2cm, measured with a ruler
2. $L/D = \log_{10}(f_p)$
3. $f_P = 10^{(L/D)} = 10^{(1cm/2cm)} = 3.16$
4. Adjust for the decade range (for this example, $f_p = 31.6$ Hz)

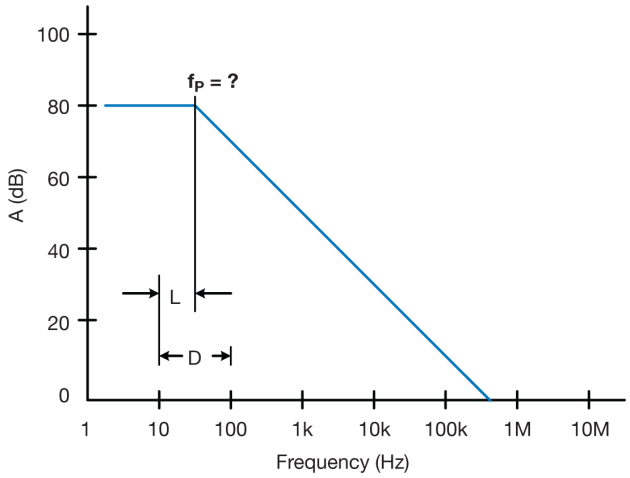


Figure 23. *Finding values on logarithmic axis not directly on a grid line*

Time to phase shift

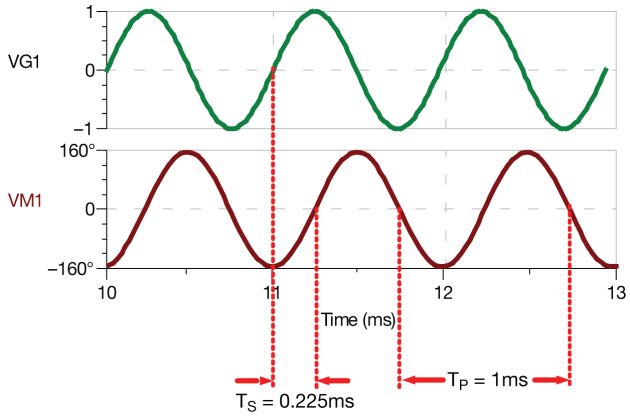


Figure 24. *Time to phase shift*

Phase shift from time

$$\theta = \frac{T_S}{T_P} \times 360^\circ \tag{66}$$

Where

T_S = time shift from input to output signal

T_P = period of signal

θ = phase shift of the signal from input to output

Example

Calculate the phase shift in degrees for **Figure 26**.

Answer

$$\theta = \frac{T_S}{T_P} \cdot 360^\circ = \left(\frac{0.225\ \text{ms}}{1\ \text{ms}}\right) \cdot 360^\circ = 81^\circ \tag{67}$$

Bode plots: Poles

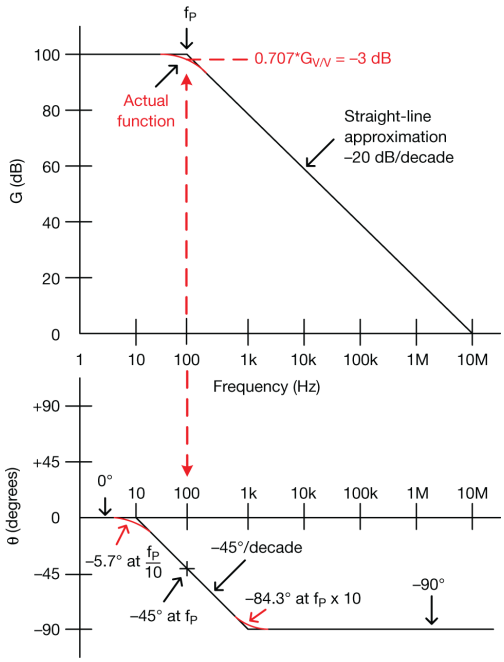


Figure 25. *Pole gain and phase*

Where

Pole location = f_P (cutoff freq)

Magnitude ($f < f_P$) = G_{DC} (for example, 100 dB)

Magnitude ($f = f_P$) = –3 dB

Magnitude ($f > f_P$) = –20 dB/decade

Phase ($f = f_P$) = –45°

Phase ($0.1\ f_P < f < 10\ f_P$) = –45°/decade

Phase ($f > 10\ f_P$) = –90°

Phase ($f < 0.1\ f_P$) = 0°

Pole (equations)

As a complex number

$$G_V = \frac{V_{OUT}}{V_{IN}} = \frac{G_{DC}}{j\left(\frac{f}{f_P}\right) + 1} \tag{68}$$

Magnitude

$$G_V = \frac{V_{OUT}}{V_{IN}} = \frac{G_{DC}}{\sqrt{\left(\frac{f}{f_P}\right)^2 + 1}} \tag{69}$$

Phase shift

$$\theta = -\tan^{-1}\left(\frac{f}{f_P}\right) \tag{70}$$

Magnitude in dB

$$G_{dB} = 20\,\mathrm{Log}(G_V) \tag{71}$$

Where

G_v = voltage gain in V/V

G_{dB} = voltage gain in decibels

G_{DC} = the dc or low frequency voltage gain

f = frequency in Hz

f_P = frequency at which the pole occurs

θ = phase shift of the signal from input to output

j = indicates imaginary number or $\sqrt{-1}$

Bode plots (zeros)

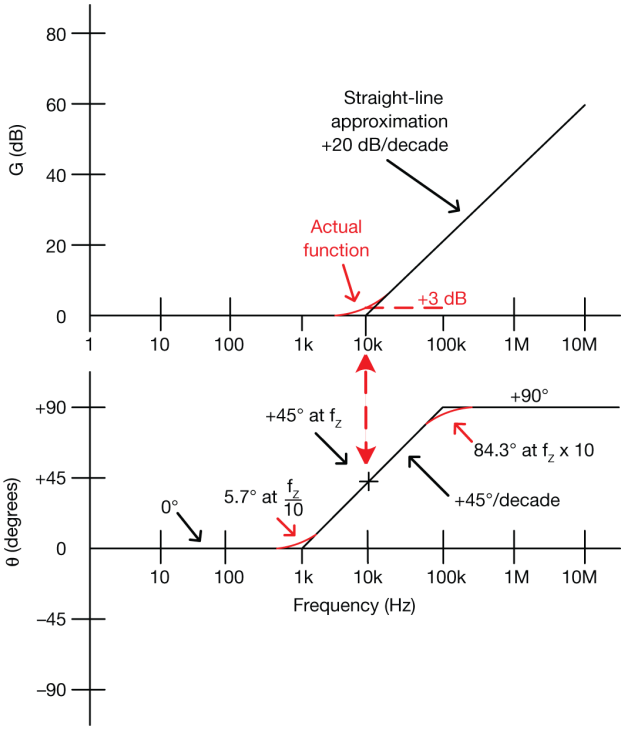


Figure 26. *Zero gain and phase*

Where

Zero location = f_Z

Magnitude ($f < f_Z$) = 0 dB

Magnitude ($f = f_Z$) = +3 dB

Magnitude ($f > f_Z$) = +20 dB/decade

Phase ($f = f_Z$) = +45°

Phase ($0.1\ f_Z < f < 10\ f_Z$) = +45°/decade

Phase ($f > 10\ f_Z$) = +90°

Phase ($f < 0.1\ f_Z$) = 0°

Zero (equations)

As a complex number

$$G_V = \frac{V_{OUT}}{V_{IN}} = \frac{G_{DC}}{j\left(\frac{f}{f_P}\right) + 1} \quad (72)$$

Magnitude

$$G_V = \frac{V_{OUT}}{V_{IN}} = \frac{G_{DC}}{\sqrt{\left(\frac{f}{f_P}\right)^2 + 1}} \quad (73)$$

Phase shift

$$\theta = -\tan^{-1}\left(\frac{f}{f_P}\right) \quad (74)$$

Magnitude in dB

$$G_{dB} = 20\,\mathrm{Log}(G_V) \quad (75)$$

Where

G_V = voltage gain in V/V

G_{dB} = voltage gain in decibels

G_{DC} = the dc or low frequency voltage gain

f = frequency in Hz

f_Z = frequency at which the zero occurs

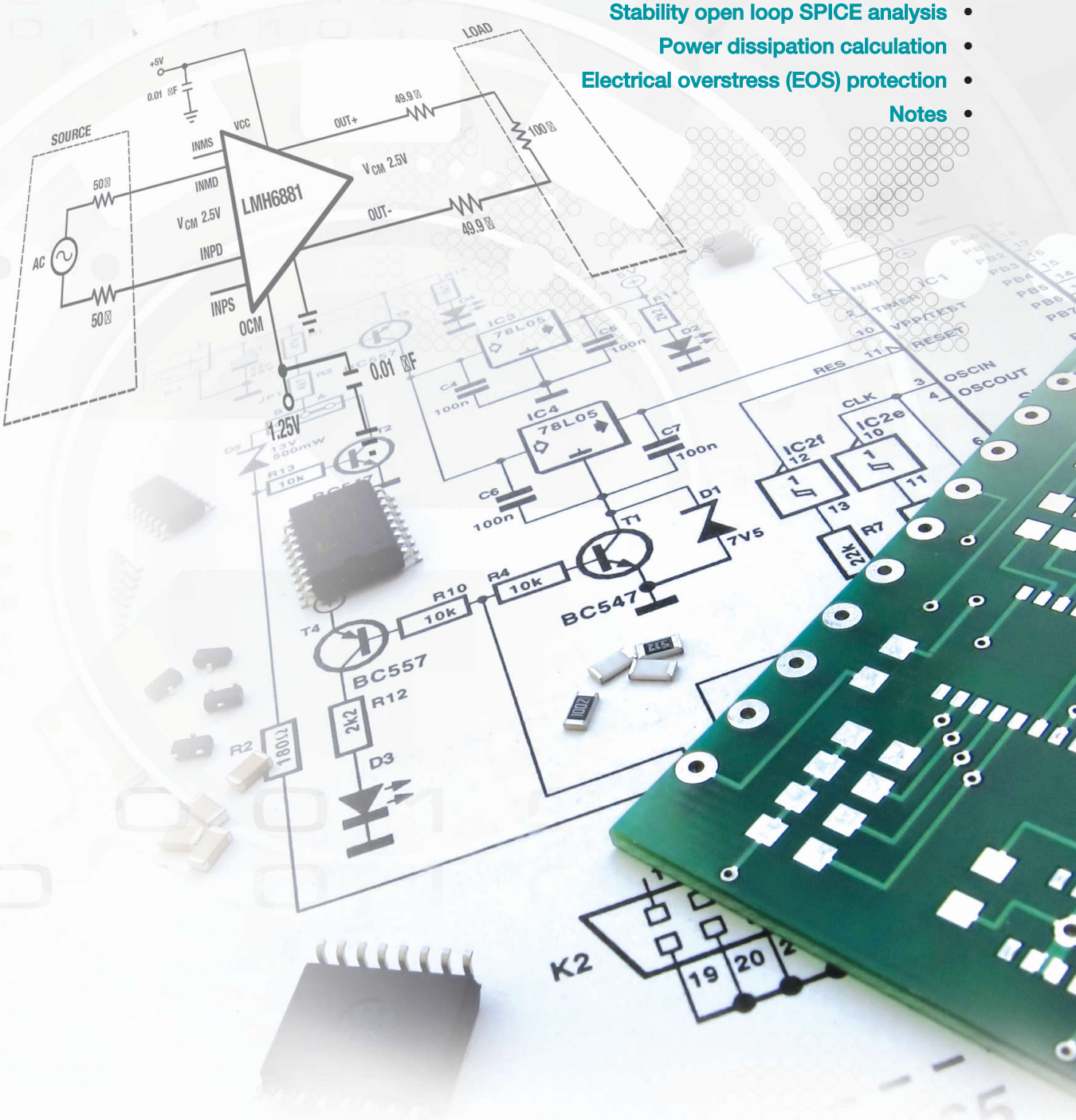
θ = phase shift of the signal from input to output

j = indicates imaginary number or $\sqrt{-1}$

Notes

Amplifier

- Basic op amp configurations
- Op amp bandwidth
- Full power bandwidth
- Large signal response (slew rate)
- Settling Time
- Combining noise sources
- AC response versus frequency (dominant 2-pole system)
- Stability open loop SPICE analysis
- Power dissipation calculation
- Electrical overstress (EOS) protection
- Notes



Basic op amp configurations

Gain for buffer configuration

$$G_{CL} = 1 \tag{76}$$

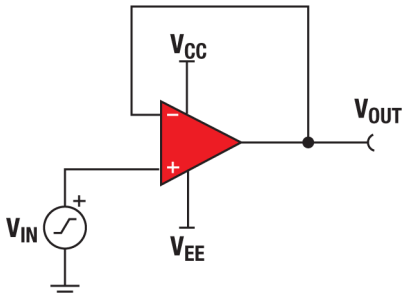


Figure 27. *Buffer configuration*

Gain for non-inverting configuration

$$G_{CL} = \frac{R_f}{R_1} + 1 \tag{77}$$

Input impedance. See data sheet for value, but typically greater than 100MΩ to 100TΩ.

$$Z_{in} = \text{Op amp input impdeance} \tag{78}$$

The common mode voltage is equal to the input signal. Check for common mode limitations.

$$V_{cm} = V_{IN} \tag{79}$$

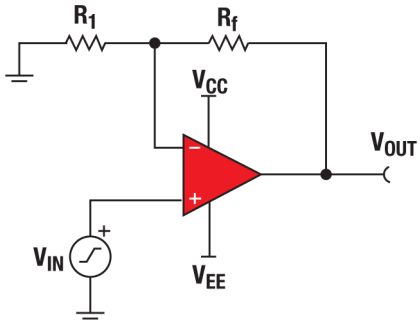


Figure 28. *Non-inverting configuration*

Gain for inverting configuration

$$G_{CL} = -\frac{R_f}{R_1} \tag{80}$$

Input impedance. Low compared to the non-inverting configuration.

$$Z_{in} = R_1 \tag{81}$$

The common mode voltage held constant at 0V so the common mode range and CMRR is not a concern

$$V_{cm} = 0V \tag{82}$$

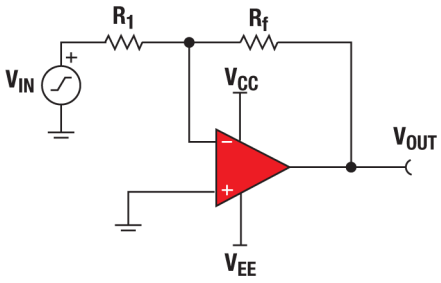


Figure 29. *Inverting configuration*

Transfer function for inverting summing amplifier

$$V_{OUT} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + ... + \frac{V_N}{R_N}\right) \tag{83}$$

Transfer function for inverting summing amplifier, assuming $R_1 = R_2 = ... = R_N$

$$V_{OUT} = -\frac{R_f}{R_1}(V_1 + V_2 + ... + V_N) \tag{84}$$

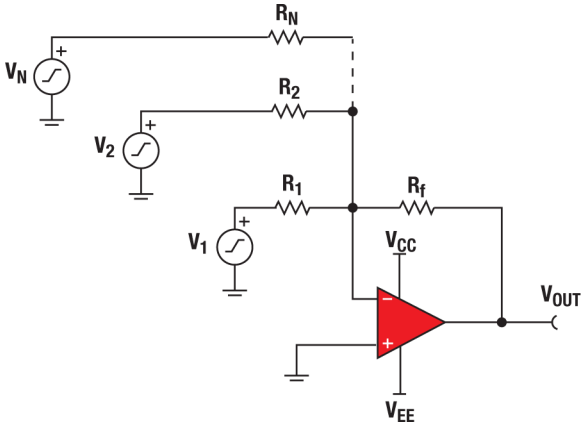


Figure 30. *Inverting summing configuration*

Transfer function for noninverting summing amplifier for equal input resistors

$$V_{OUT} = \left(\frac{R_f}{R_{in}} + 1\right)\left[\frac{V_1}{N} + \frac{V_2}{N} + ... + \frac{V_N}{N}\right] \tag{85}$$

Where

$R_1 = R_2 = ... = R_N$

N = number of input resistors

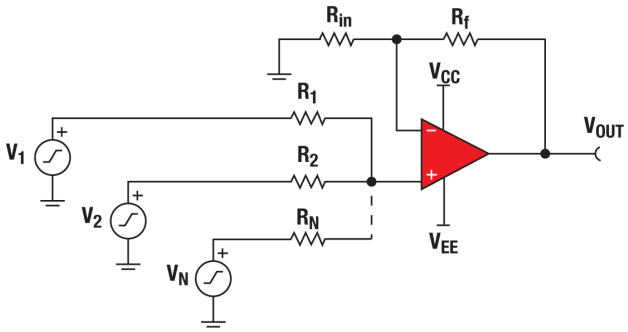


Figure 31. *Non-inverting summing configuration*

Simple non-inverting amp with C_f filter

Gain for non-inverting configuration for f < f_C

$$G_{LF} = \frac{R_f}{R_1} + 1 \tag{86}$$

Gain for non-inverting configuration for f >> f_C

$$G_{HF} = 1 \tag{87}$$

Cut off frequency for non-inverting configuration

$$f_C = \frac{1}{2\pi R_f C_f} \tag{88}$$

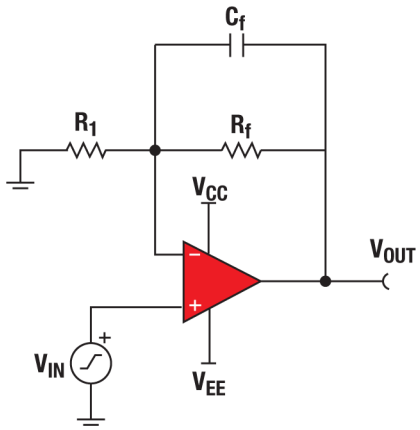


Figure 32. *Non-inverting amplifier with C_f filter*

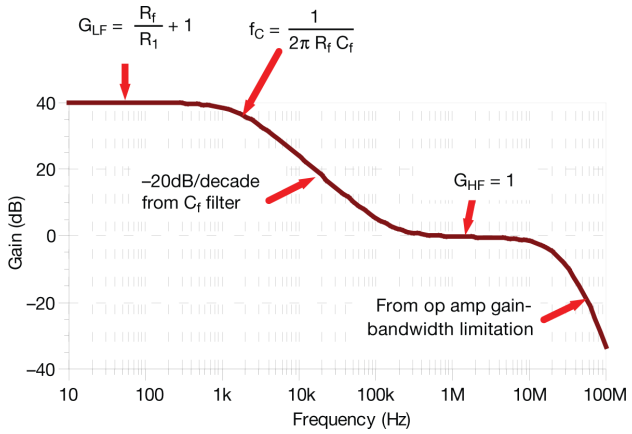


Figure 33. *Frequency response for non-inverting op amp with C_f filter*

Simple inverting amp with C_f filter

Gain for inverting configuration for f < f_C

$$G_{LF} = -\frac{R_f}{R_1} \tag{89}$$

Gain for inverting configuration for f > f_C

$$G_{HF} = -20\text{dB/decade after } f_C \text{ until op amp bandwidth limitation} \tag{90}$$

Cutoff frequency for inverting configuration

$$f_C = \frac{1}{2\pi R_f C_f} \tag{91}$$

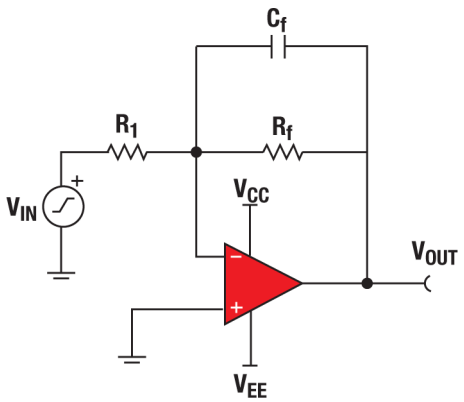


Figure 34. *Inverting amplifier with C_f filter*

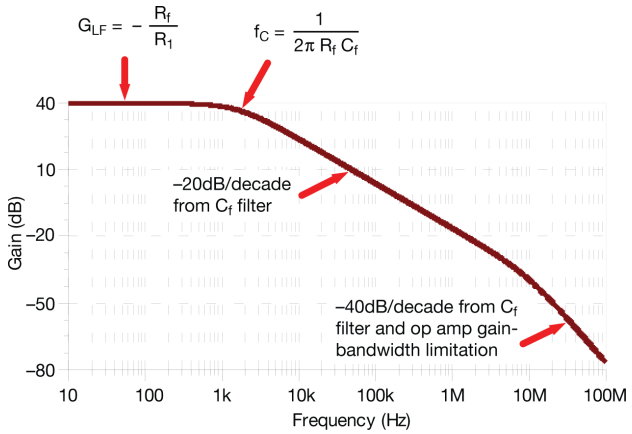


Figure 35. *Frequency response for inverting op amp with C_f filter*

Differential filter cutoff

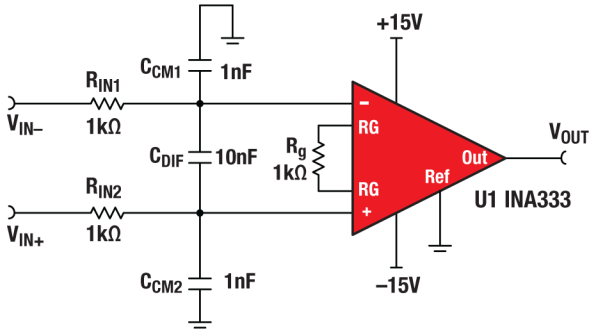


Figure 36. *Input filter for instrumentation amplifier*

Differential capacitor is sized 10 times the common-mode capacitor

$$\text{Select } C_{DIF} \geq 10C_{CM1} \tag{92}$$

Input resistors must be equal

$$R_{IN1} = R_{IN2} \tag{93}$$

Common-mode capacitors must be equal

$$C_{CM1} = C_{CM2} \tag{94}$$

Common-mode filter cutoff

$$f_{CM} = \frac{1}{2\pi R_{IN1} C_{CM1}} \tag{95}$$

Differential filter cutoff

$$f_{DIF} = \frac{1}{2\pi(2R_{IN1})\left(C_{DIF} + \frac{1}{2}C_{CM1}\right)} \tag{96}$$

Where

f_{DIF} = differential cutoff frequency

f_{CM} = common-mode cutoff frequency

R_{IN} = input resistance

C_{CM} = common-mode filter capacitance

C_{DIF} = differential filter capacitance

Note

Selecting $C_{DIF} \geq 10\ C_{CM}$ sets the differential mode cutoff frequency about 20 times lower than the common-mode cutoff frequency. This prevents common-mode noise from being converted into differential noise due to component tolerances.

Calculating amplifier offset voltage

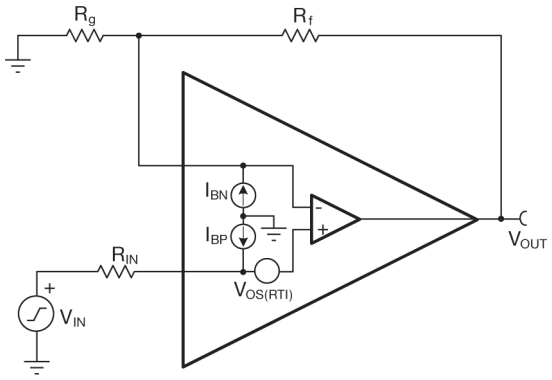


Figure 37. *Op amp bias current and offset calculations*

Equivalent feedback resistance

$$R_{eq} = \frac{R_f \cdot R_g}{R_f + R_g} \tag{97}$$

Offset RTI from I_{BN} flowing into feedback

$$V_{OS(IBN)} = I_{BN} \cdot R_{eq} \tag{98}$$

Offset RTI from I_{BP} flowing into source impedance

$$V_{OS(IBP)} = I_{BP} \cdot R_{IN} \tag{99}$$

Directly adding the offset components. Conservative estimate.

$$V_{OS(\text{total worst})} = \pm V_{OS(Amp)} \pm V_{OS(BN)} \pm V_{OS(IBP)} \tag{100}$$

Statistically adding the offset components. More realistic estimate.

$$V_{OS(\text{total stat})} = \sqrt{V_{OS(Amp)}^2 + V_{OS(IBN)}^2 + V_{OS(IBP)}^2} \tag{101}$$

Noise gain of op amp (always non-inverting gain)

$$G_n = \frac{R_f}{R_g} + 1 \tag{102}$$

Offset referred to the output

$$V_{OS(RTO)} = V_{OS(RTI)} \cdot G_n \tag{103}$$

Where

R_f, R_g = the feedback and gain setting resistors

R_{IN} = resistance seen by noninverting input

I_{BN}, I_{BP} = the current flowing from the inverting (I_{BN}) and noninverting (I_{BP}) op amp input as specified in the data sheet

$V_{os(amp)}$ = the input offset voltage specification from the op amp data sheet

$V_{OS(RTI)}$ = this is the offset referred to the input. This can be either $V_{os(total\ worst)}$ or $V_{os(total\ stat)}$.

Op amp bandwidth

Gain bandwidth product defined

$$GBW = G_n \cdot BW \tag{104}$$

Where

GBW = gain bandwidth product, listed in op amp data sheet specification table

G_n = closed loop noise gain, always non-inverting gain

BW = the bandwidth limitation of the amplifier

Example

Determine bandwidth using **Equation 99**, where

G_n = 100 (from amplifier configuration)

GBW = 22MHz (from data sheet)

Answer

$$BW = \frac{GBW}{G_n} = \frac{22MHz}{100} = 220kHz \tag{105}$$

Note that the same result can be graphically determined using the A_{OL} curve as shown below.

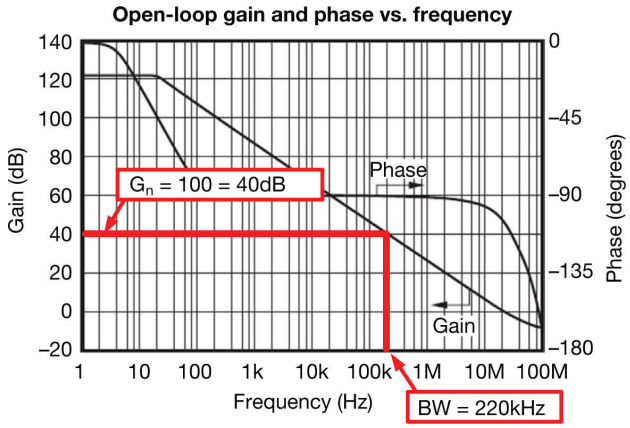


Figure 38. *Using A_{OL} to find closed-loop bandwidth*

Small signal step response

Rise time for a small signal step

$$\tau_R = \frac{0.35}{f_C} \tag{106}$$

Where

τ_R = the rise time of a small signal step response

f_C = the closed-loop bandwidth of the op amp circuit

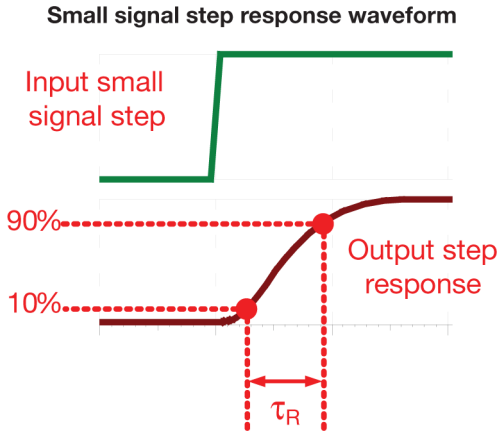


Figure 39. *Small signal step response*

Full power bandwidth

Maximum output without slew-rate induced distortion

$$V_P = \frac{SR}{2\pi f} \tag{107}$$

Where

V_P = maximum peak output voltage before slew induced distortion occurs

SR = slew rate

f = frequency of applied signal

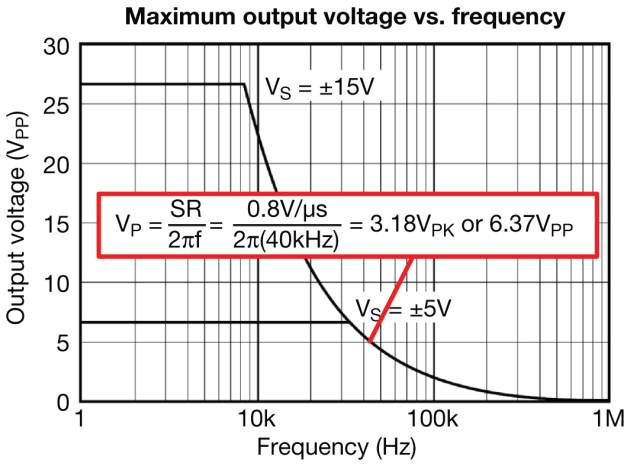


Figure 40. *Maximum output without slew-rate induced distortion*

Notice that the above figure is graphed using **Equation 100** for the OPA277. The example calculation shows the peak voltage for the OPA277 at 40kHz. This can be determined graphically or with the equation.

Example

$$V_P = \frac{SR}{2\pi f} = \frac{0.8V/\mu s}{2\pi(40kHz)} = 3.18V_{PK} \text{ or } 6.37V_{PP} \quad (108)$$

Large signal response (slew rate)

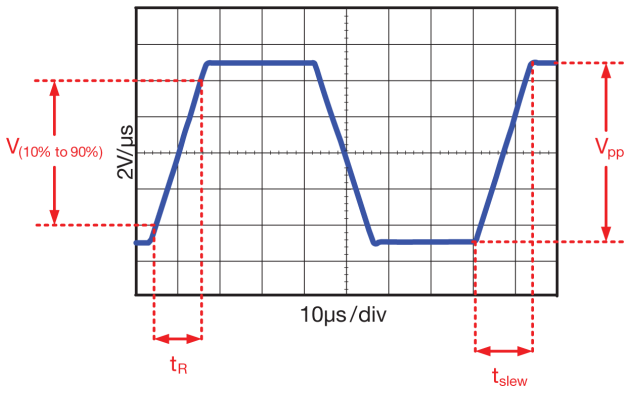


Figure 41. *Large signal step response*

Rise time for large signal step response

$$t_R = \frac{V_{(10\% \text{ to } 90\%)}}{SR} \quad (109)$$

Approximate total time for waveform to transition from peak to peak for large signal response

$$t_{slew} \approx \frac{V_{pp}}{SR} \quad (110)$$

Where

$V_{(10\% \text{ TO } 90\%)}$ = the change in output voltage from 10% to 90% for a step input

SR = the slew rate of the amplifier

V_{pp} = peak-to-peak square wave voltage for a step response

Settling Time

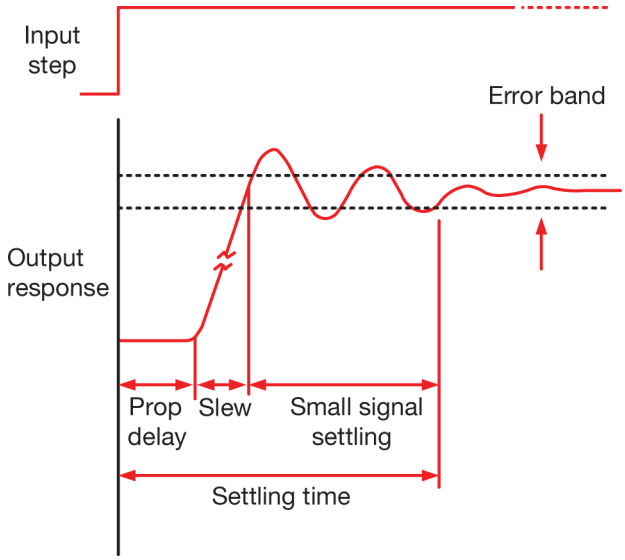


Figure 42. *Small signal step response*

Where

Settling time = the time from when an input step is applied until the output settles inside an error guard band. Settling time is measured with a large step (near full scale) input.

Prop delay = propagation delay. The time from when the input step is applied until the output begins to respond

Slew = the output is transitioning at the maximum rate given by the slew rate specification in the amplifier data sheet

Combining noise sources

Combining two uncorrelated noise sources

$$e_{nT} = \sqrt{(e_{n1})^2 + (e_{n2})^2} \tag{111}$$

Combining two correlated noise sources

$$e_{nT} = \sqrt{(e_{n1})^2 + (e_{n2})^2 + 2 \cdot C \cdot e_{n1} \cdot e_{n2}} \tag{112}$$

Where

e_{nT} = total noise

e_{n1}, e_{n2} = noise sources

C = correlation factor, ranges from -1 to +1. C= 0 for uncorrelated sources, C=-1 for inversely correlated, and C=+1 for directly correlated.

Averaging noise sources

Averaging noise

$$e_{nAvg} = \frac{e_n}{\sqrt{N}} \tag{113}$$

Where

e_{nAvg} = the noise amplitude after averaging

e_n = the noise amplitude before averaging

N = the number of averages

Noise bandwidth calculation

Noise bandwidth

$$BW_n = K_n \cdot f_c \tag{114}$$

Where

BW_n = noise bandwidth of the system

K_n = the brick wall correction factor for different filter order

f_c = –3 dB bandwidth of the system

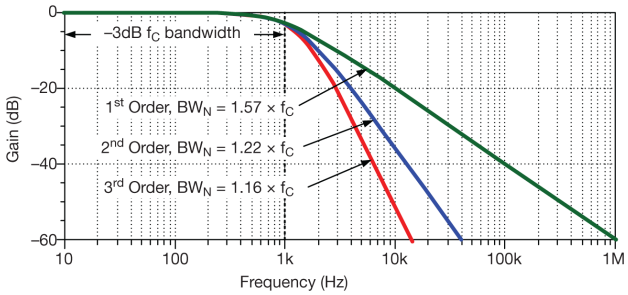


Figure 43. *Op amp bandwidth for three different filter orders*

Table 17. Brick wall correction factors for noise bandwidth

Number of poles	K_n brick wall correction factor
1	1.57
2	1.22
3	1.13
4	1.12

Broadband total noise calculation

$$E_{n(BB)} = e_n \cdot \sqrt{BW_n} \tag{115}$$

Figure 44. *Total RMS noise from broadband*

Where

$E_{n(BB)}$ = total RMS noise from broadband noise

e_n = broadband noise spectral density ($nV/\sqrt{Hz}$)

BW_n = noise bandwidth (Hz)

1/f total noise calculation

Normalized 1/f noise at 1 Hz

$$E_{n(normal)} = e_{n(flicker)}\sqrt{f_o} \tag{116}$$

Where

$E_{n(normal)}$ = 1/f noise normalized to 1 Hz

$e_{n(flicker)}$ = noise spectral density measured in the 1/f region

f_o = the frequency at which the 1/f noise $e_{n(flicker)}$ is measured

1/f total noise calculation

$$E_{n(flicker)} = E_{n(normal)}\sqrt{\ln\left(\frac{f_H}{f_L}\right)} \tag{117}$$

Where

$E_{n(flicker)}$ = total RMS noise from flicker

$E_{n(normal)}$ = 1/f noise normalized to 1Hz

f_H = upper cutoff frequency or noise bandwidth

f_L = lower cutoff frequency, normally set to 0.1Hz

Table 18. Peak-to-peak conversion

Number of standard deviations	Percent chance reading is in range
2σ (same as ±1σ)	68.3%
3σ (same as ±1.5σ)	86.6%
4σ (same as ±2σ)	95.4%
5σ (same as ±2.5σ)	98.8%
6σ (same as ±3σ)	99.7%
6.6σ (same as ±3.3σ)	99.9%

Thermal noise calculation

Total RMS thermal noise

$$E_{n(R)} = \sqrt{4 \cdot k \cdot T_K \cdot R \cdot BW_n} \quad (118)$$

Thermal noise spectral density

$$e_{n(R)} = \sqrt{4 \cdot k \cdot T_K \cdot R} \quad (119)$$

Where

$E_{n(R)}$ = total RMS noise from resistance, also called thermal noise (V RMS)

$e_{n(R)}$ = noise spectral density from resistance, also called thermal noise ($V/\sqrt{Hz}$)

k = Boltzmann's constant 1.38 x 10^{-23}J/K

T_K = temperature in Kelvin, to convert degrees Celsius to Kelvin $T_K = T_c + 273.15$

BW_n = noise bandwidth in Hz

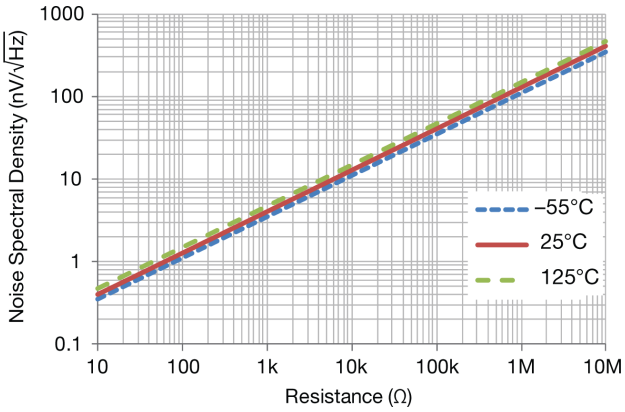


Figure 45. *Noise spectral density vs. resistance*

Op amp noise model

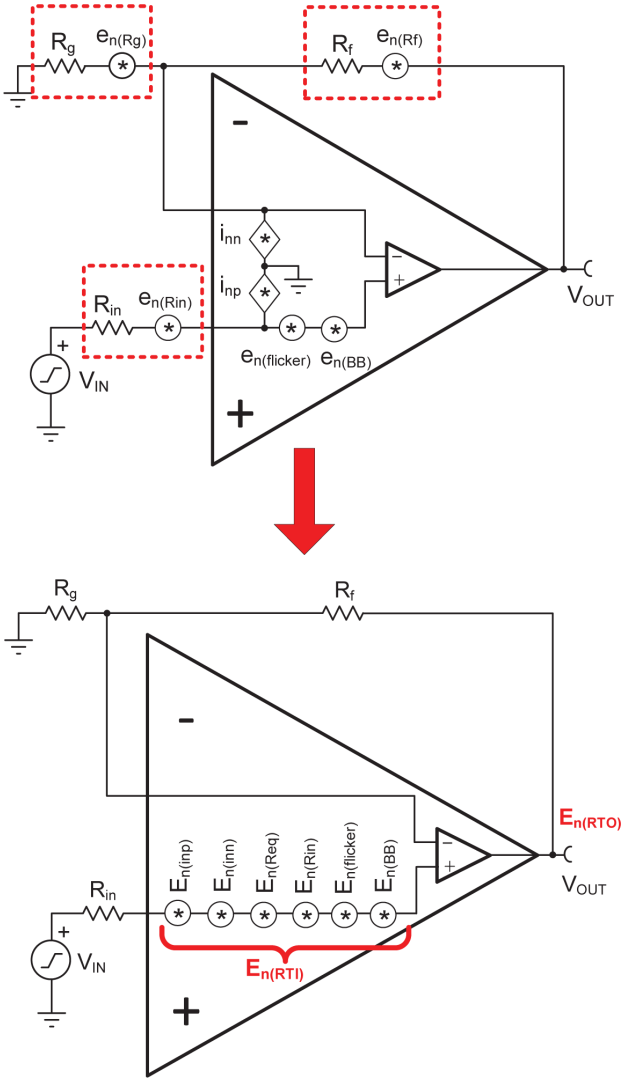


Figure 46. *Op amp noise model*

Total noise calculations

Equivalent feedback resistance

$$R_{eq} = \frac{R_f \cdot R_g}{R_f + R_g} \tag{120}$$

Noise RTI from i_{nn} flowing into feedback resistors

$$e_{n(inn)} = i_{nn} \cdot R_{eq} \tag{121}$$

Noise RTI from i_{np} flowing into input resistance

$$e_{n(inp)} = i_{np} \cdot R_{in} \tag{122}$$

Thermal noise RTI from feedback network

$$e_{n(Req)} = \sqrt{4 \cdot k \cdot T_K \cdot R_{eq}} \tag{123}$$

Thermal noise RTI from input resistor

$$e_{n(Rin)} = \sqrt{4 \cdot k \cdot T_K \cdot R_{in}} \tag{124}$$

Broadband noise from data sheet

$$e_{n(BB)} \tag{125}$$

General equation to convert spectral density to RMS

$$E_n = e_n \cdot \sqrt{BW_n} \tag{126}$$

Flicker noise normalized to 1Hz

$$E_{n(normal)} = e_{n(flicker)}\sqrt{f_o} \tag{127}$$

Op amp RMS flicker noise

$$E_{n(flicker)} = E_{n(normal)} \cdot \sqrt{\ln\left(\frac{f_H}{f_L}\right)} \tag{128}$$

Total noise RTI

$$E_{n(RTI)} = \sqrt{E_{n(BB)}^2 + E_{n(flicker)}^2 + E_{n(Rin)}^2 + E_{n(Req)}^2 + E_{n(inp)}^2 + E_{n(inn)}^2} \tag{129}$$

Noise gain

$$G_n = \frac{R_f}{R_g} + 1 \tag{130}$$

Total noise RTO

$$E_{n(RTO)} = E_{n(RTI)} \cdot G_n \tag{131}$$

Note

1. equations above were defined previously
2. capital letter (e.g. “E”) indicates RMS noise, and lowercase letter (e.g. “e”) indicate noise density (e.g. V / $\sqrt{Hz}$)

RTO = referred to the output

RTI = referred to the input

AC response versus frequency (dominant 2-pole system)

Figure 46 illustrates a bode plot with four different examples of AC peaking.

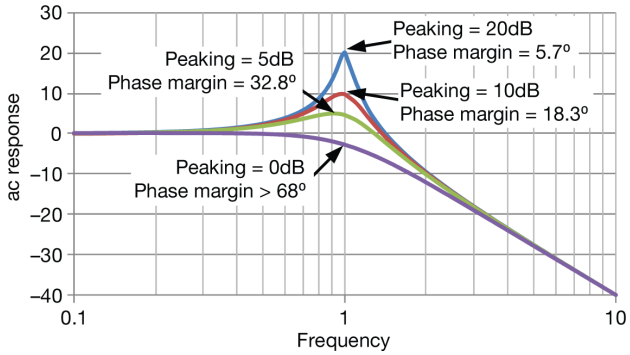


Figure 47. *Stability – AC peaking relationship example*

Phase margin versus AC peaking

This graph illustrates the phase margin for any given level of AC peaking. Note that 45° of phase margin or greater is required for stable operation.

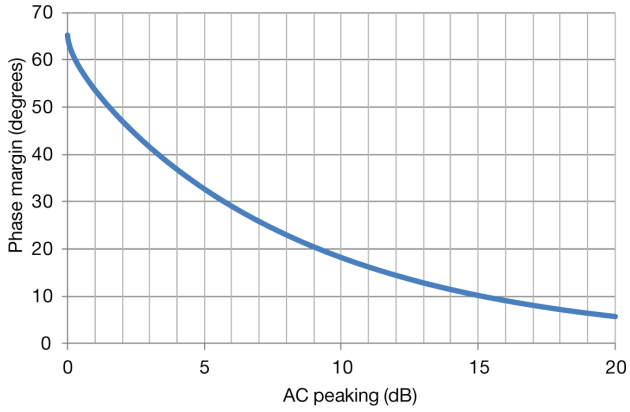


Figure 48. *Stability – phase margin vs. peaking for a two-pole system*

Transient overshoot (dominant 2-pole system)

Figure 49 illustrates a transient response with two different examples of percentage overshoot.

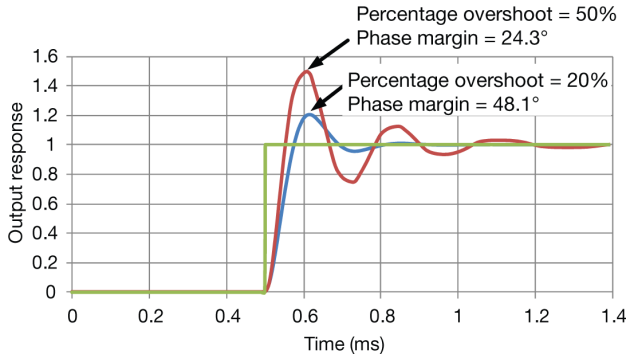


Figure 49. *Stability – transient overshoot example*

Phase margin versus percentage overshoot

This graph illustrates the phase margin for any given level of transient overshoot. Note that 45° of phase margin or greater is required for stable operation.

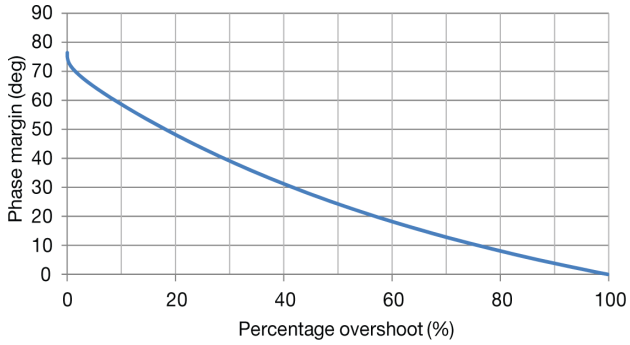


Figure 50. *Stability – phase margin vs. percentage overshoot*

Stability open loop SPICE analysis

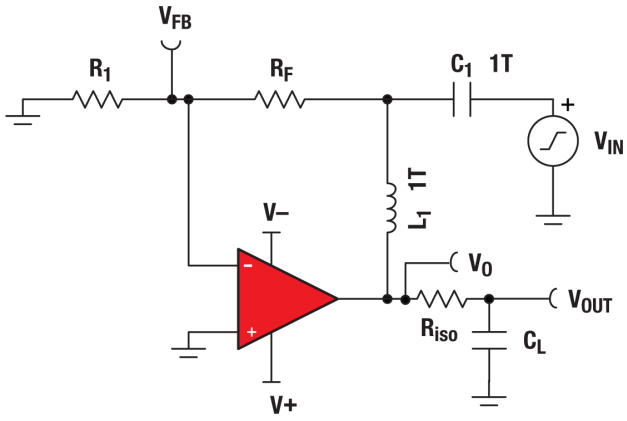


Figure 51. *Common spice test circuit used for stability*

Loaded open-loop gain

$$A_{OL\_LOADED} = \frac{V_O}{V_{FB}} \tag{132}$$

Feedback factor

$$\beta = V_{FB} \tag{133}$$

Closed-loop noise gain

$$\frac{1}{\beta} = \frac{1}{V_{FB}} \tag{134}$$

Loop gain

$$A_{OL\_LOADED} \times \beta = V_O \tag{135}$$

Where

V_O = the voltage at the output of the op amp

V_{OUT} = the voltage output delivered to the load, which may be important to the application but is not considered in stability analysis

V_{FB} = feedback voltage

R_F, R_1, R_{iSO} and C_L = the op amp feedback network and load. Other op amp topologies will have different feedback networks; however, the test circuit will be the same for most cases. **Figure 50** shows the exception to the rule (multiple feedback).

C_1 and L_1 = components that facilitate SPICE analysis. They are large (1TF, 1TH) to make the circuit closed-loop for DC, but open loop for AC frequencies. SPICE requires closed-loop operation at DC for convergence.

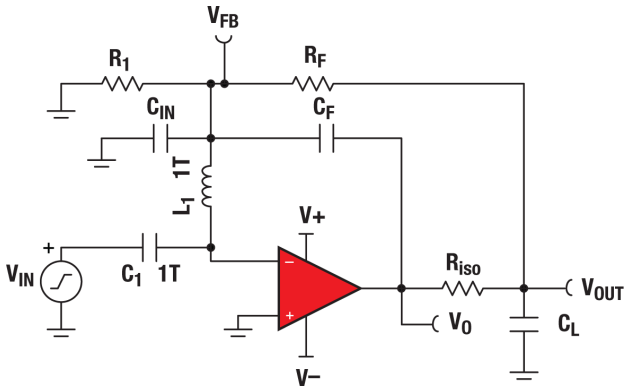


Figure 52. *Alternative (multiple feedback) SPICE test circuit used for stability*

Loaded open loop gain

$$A_{OL\_LOADED} = V_O \tag{136}$$

Feedback factor

$$\beta = \frac{V_{FB}}{V_O} \tag{137}$$

Closed-loop noise gain

$$\frac{1}{\beta} = \frac{V_O}{V_{FB}} \tag{138}$$

Loop gain

$$A_{OL\_LOADED} \times \beta = V_{FB} \tag{139}$$

Where

V_O = the voltage at the output of the op amp

V_{OUT} = the voltage output delivered to the load. This may be important to the application but is not considered in stability analysis.

V_{FB} = feedback voltage

R_F, R_1, R_{iso} and C_F = the op amp feedback network. Because there are two paths for feedback, the loop is broken at the input.

C_1 and L_1 = components that facilitate SPICE analysis. They are large (1TF, 1TH) to make the circuit closed loop for DC, but open loop for AC frequencies. SPICE requires closed-loop operation at DC for convergence.

C_{IN} = the equivalent input capacitance taken from the op amp datasheet. This capacitance normally does not need to be added because the model includes it. However, when using this simulation method the capacitance is isolated by the 1TH inductor.

Stability transient square wave lab test

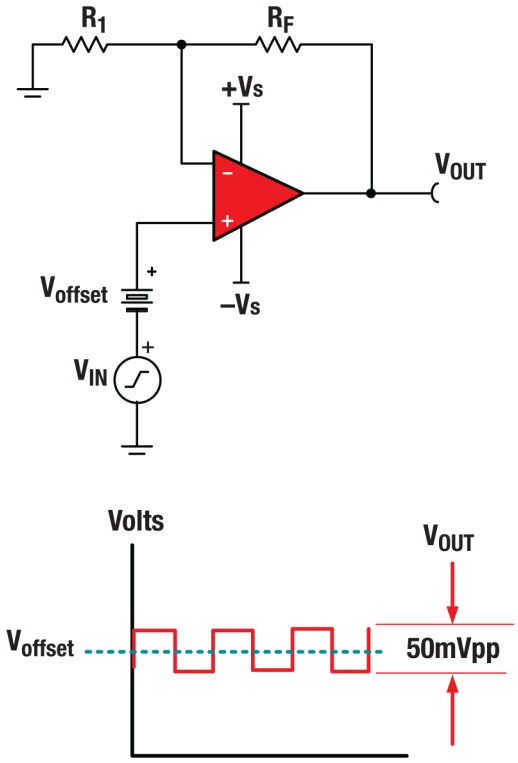


Figure 53. *Transient real world stability test*

Test tips

- Choose test frequency << f_{cl}
- Small signal (Vpp ≤ 50 mV) ac output square wave (for example, 1 kHz)
- Adjust V_{IN} amplitude to yield output ≤ 50 mVpp
- Worst case is usually when V_{offset} = 0 (largest R_O, for I_{OUT} = 0A)
- Use V_{offset} as desired to check all output operating points for stability

- Set scope = AC coupled and expand vertical scope scale to look for amount of overshoot, undershoot, and ringing on V_{OUT}
- Use 1x attenuation scope probe on V_{OUT} for best resolution
- Use percentage overshoot to determine phase margin using **Figure 50**

Stability AC sine wave lab test

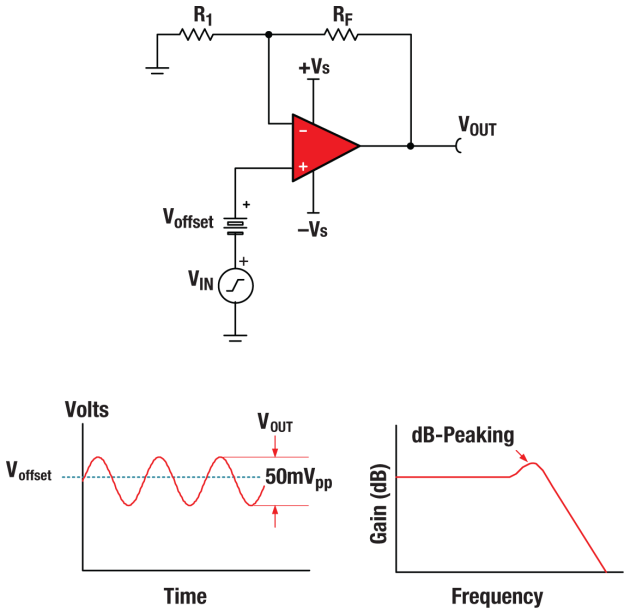


Figure 54. *AC sweep real world stability test*

Test tips

- Small signal (Vpp ≤ 50 mV) AC output sine wave
- Adjust V_{IN} amplitude to yield output ≤ 50 mVpp
- Worst case is usually when V_{offset} = 0 (largest R_O, for I_{OUT} = 0A)
- Use V_{offset} as desired to check all output operating points for stability
- Sweep input frequency or use network analyzer to automatically sweep frequency
- Use AC coupling
- Use 1x attenuation scope probe on V_{OUT} for best resolution
- Use AC peaking in decibels to determine phase margin using **Figure 48**

Power dissipation calculation

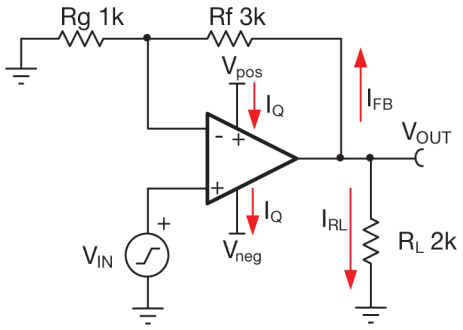


Figure 55. *Current and power dissipation for non-inverting amplifier*

Non-inverting amplifier power dissipation for specific V_{OUT}

Current through load resistor

$$I_{RL} = \frac{V_{OUT}}{R_L} \tag{140}$$

Current through feedback network

$$I_{FB} = \frac{V_{OUT}}{R_F + R_g} \tag{141}$$

Power dissipated inside op amp from load current.

$$P_L = (|I_{RL}| + |I_{FB}|)\left(|V_{sup}| - |V_{OUT}|\right) \tag{142}$$

$V_{sup} = V_{pos}$ if the amplifier is sourcing.

$V_{sup} = V_{neg}$ if the amplifier is sinking.

Total power from quiescent current

$$P_Q = \left(V_{pos} - V_{neg}\right) \cdot I_Q \tag{143}$$

Total power dissipated inside the op amp

$$P_T = P_L + P_Q \tag{144}$$

Non-inverting amplifier maximum power dissipation

Equivalent load resistance

$$R_{L\_EQ} = (R_L)\,||\left(R_g + R_F\right) \tag{145}$$

Maximum DC power dissipation inside the amplifier. Max power occurs when V_{OUT}= ½ V_{sup}. V_{sup} = V_{pos} = |V_{neg}| for a dual symmetrical supply. V_{sup} = V_{pos} for single supply configuration.

$$P_{dc\_max} = \frac{V_{sup}^2}{4 \cdot R_{L\_EQ}} \tag{146}$$

Maximum AC average power dissipation for a sinusoidal signal on dual supply configuration. Max average power occurs when the V_{OUT_pk} = (2·Vcc/π). V_{sup} = V_{pos} = V_{neg} for a dual symmetrical supply. For single supply max average AC power is equal to Pdc_max. This assumes sinewave is centered at mid-supply.

$$P_{ac\_max\_avg} = \frac{2 \cdot V_{sup}^2}{\pi^2 \cdot R_{L\_EQ}} \tag{147}$$

Junction temperature as a function of power and ambient temperature. T_j = junction temperature. θ_{ja} = junction to ambient thermal resistance. P = P_{dc_max} or $P_{ac\_max\_avg}$ depending on your application. T_a = ambient temperature.

$$T_j = \theta_{ja} \cdot P + T_a \tag{148}$$

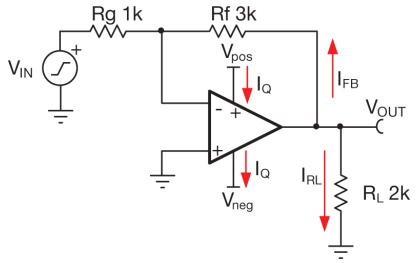


Figure 56. *Current and power dissipation for inverting amplifier*

Inverting amplifier power dissipation for specific V_{OUT}

Current through load resistor

$$I_{RL} = \frac{V_{OUT}}{R_L} \tag{149}$$

Current through feedback network

$$I_{FB} = \frac{V_{OUT}}{R_F} \tag{150}$$

Power dissipated in op amp from load current, where V_{sup} = V_{pos} if the amplifier is sourcing, or V_{neg} if the amplifier is sinking

$$P_L = (|I_{RL}| + |I_{FB}|)\left(|V_{sup}| - |V_{OUT}|\right) \tag{151}$$

Total power from quiescent current

$$P_Q = \left(V_{pos} - V_{neg}\right) \cdot I_Q \tag{152}$$

Total power dissipated inside the op amp

$$P_T = P_L + P_Q \tag{153}$$

Equivalent load resistance

$$P_{L\_EQ} = (R_L) \,||\, (R_F) \tag{154}$$

Inverting amplifier maximum power dissipation

Maximum DC power dissipation inside the amplifier. Max power occurs when V_{OUT} = ½ V_{sup}. V_{sup} = V_{pos} = $|V_{neg}|$for a dual symmetrical supply. V_{sup} = V_{pos} for single supply configuration.

$$P_{dc\_max} = \frac{V_{sup}^2}{4 \cdot R_{L\_EQ}} \tag{155}$$

Maximum AC average power dissipation for a sinusoidal signal on dual supply configuration. Max average power occurs when the V_{OUT_pk}= (2·Vcc/π). V_{sup} = V_{pos} = V_{neg} for a dual symmetrical supply. For single supply max average AC power is equal to P_{dc_max}. This assumes sinewave is centered at mid-supply.

$$P_{ac\_max\_avg} = \frac{2 \cdot V_{sup}^2}{\pi^2 \cdot R_{L\_EQ}} \tag{156}$$

Junction temperature as a function of power and ambient temperature. T_j = junction temperature. θ_{ja} = junction to ambient thermal resistance. P = P_{dc_max} or $P_{ac\_max\_avg}$ depending on your application. T_a = ambient temperature.

$$T_j = \theta_{ja} \cdot P + T_a \tag{157}$$

Electrical overstress (EOS) protection

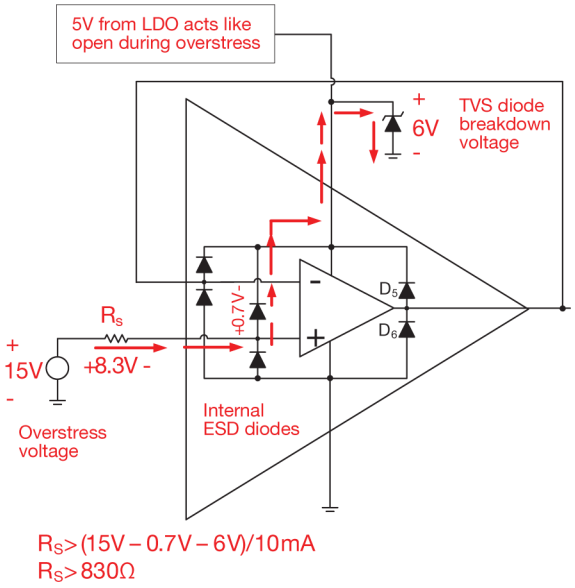


Figure 57. *EOS protection during overstress event*

Method for selecting EOS protection

1. Choose a unidirectional transient voltage suppressor (TVS) diode that has a reverse standoff equal to the normal operating supply voltage. For example, reverse standoff of V_R = 5V, for an amplifier with a 5V supply. This assures a low TVS diode leakage.
2. Try to find a TVS diode that also breaks down below the absolute maximum rating for the device that is being protected. For example, breakdown of $V_{BR} \leq 6V$ for an absolute maximum of 6V. Note that this may not always be possible. Choose the lowest breakdown available.
3. Choose a series resistor, R_s, to limit the current to the absolute maximum input current. This is commonly 10mA for many devices. $R_s > (V_{overstress} - 0.7V - V_{BR})$. For this example, $R_s = (15V - 0.7V - 6V) = 830\Omega$.
4. Increase the value of the series resistor for more design margin.

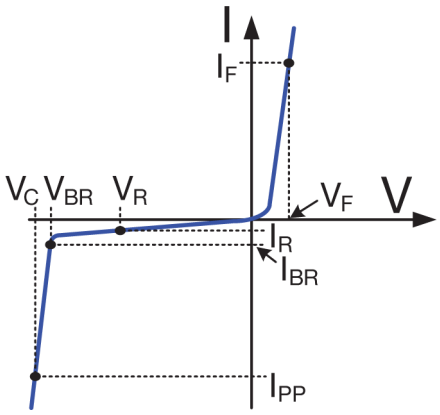


Figure 58. *Typical unidirectional TVS I-V curve*

Where

V_{BR} = breakdown voltage

V_R = stand-off voltage. The normal operating voltage with a guaranteed reverse leakage current.

V_C = clamping voltage. The voltage across the TVS when maximum current is flowing.

V_F = forward voltage drop, typically 0.7V for a unipolar TVS diode

I_{BR} = breakdown current @ V_{BR}

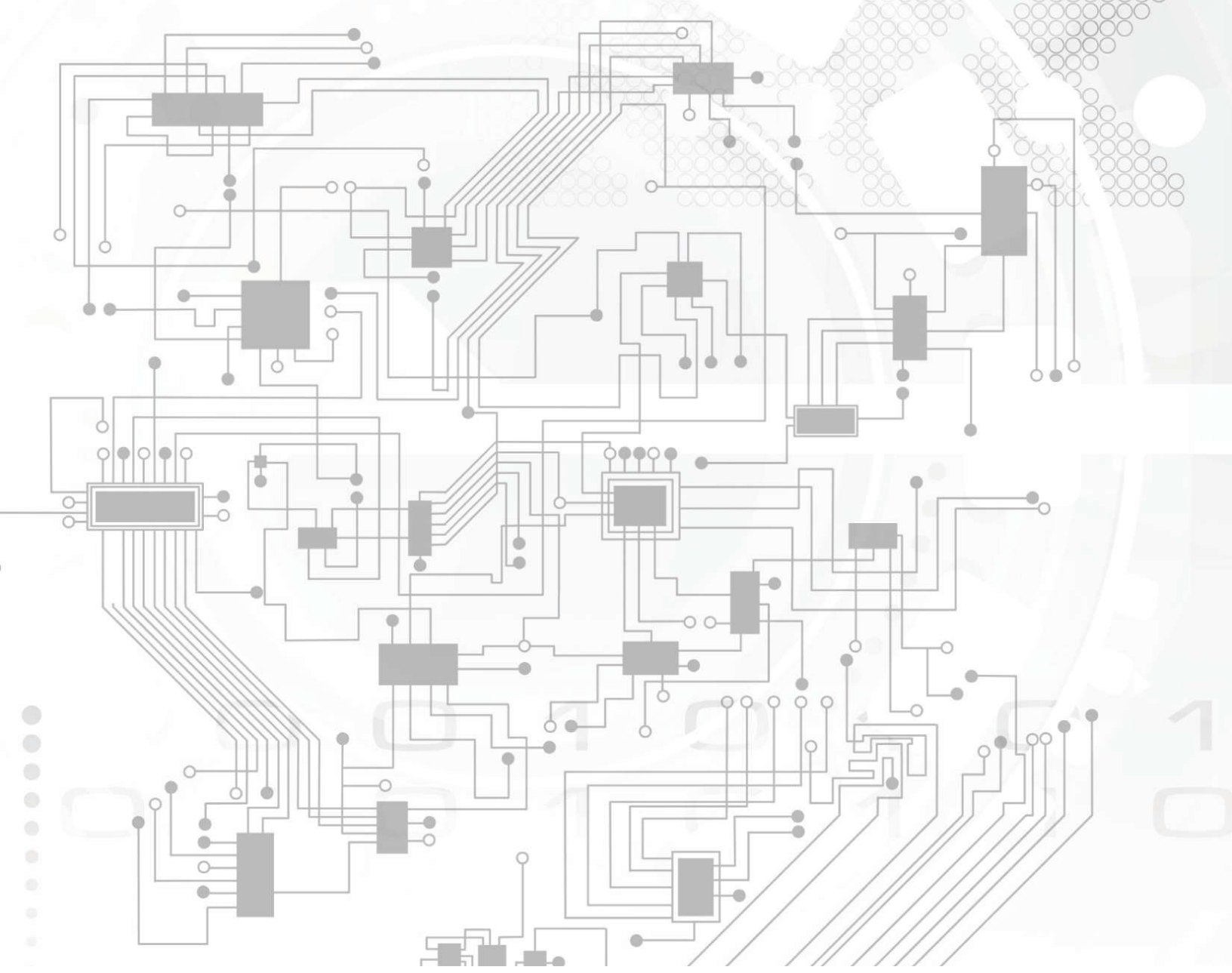
I_R = reverse leakage @ V_R. Typically in the microamps.

I_F = forward current @ V_F

I_{PP} = maximum peak pulse current @ V_C, applied for a limited time (microseconds)

Notes

PCB and Wire



PCB and Wire

Table 19. Printed circuit board conductor spacing

Voltage between conductors (DC or AC peaks)	Minimum spacing						
	Bare board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.492 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.492 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]

Where

B1 = internal conductors

B2 = external conductors uncoated sea level to 3050m

B3 = external conductors uncoated above 3050m

B4 = external conductors coated with permanent polymer coating (any elevation)

A5 = external conductors with conformal coating over assembly (any elevation)

A6 = external component lead/termination, uncoated, sea level to 3050m

A7 = external component lead termination, with conformal coating (any elevation)

Extracted with permission from IPC-2221B, **Table 6**

For additional information, the entire specification can be downloaded at

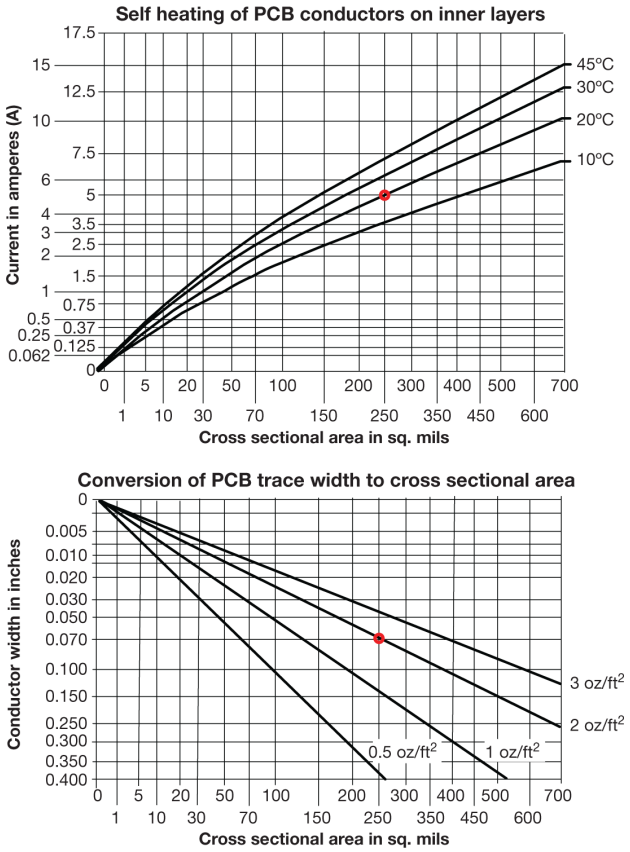


Figure 59. *Self heating of PCB traces on inside layer*

Example

Find the current that will cause a 20°C temperature rise in a PCB trace that is 0.1 inch wide and uses 2 oz/ft^2 copper. (Assume traces are on inner layer of PCB.)

Answer

First translate 0.1 inch to 250 sq. mils. using bottom chart. Next, find the current associated with 20°C and 250 sq. mils. using top chart (Answer = 5A).

Extracted with permission from IPC-2152, **Figure 5**.

For additional information the entire specification can be downloaded at **www.ipc.org**.

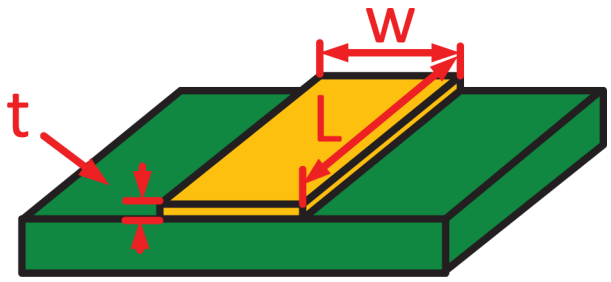


Figure 60. *PCB trace resistance*

Trace resistance

$$R = \rho\frac{L}{t \cdot W}\left[1 + \alpha\left(T - 25^{\circ}C\right)\right] \tag{158}$$

Where

ρ = resistivity of trace (for copper = $17 \cdot 10^{-6}$ Ω·mm)

α = temperature coefficient (for copper = $3.9 \cdot 10^{-3}$ /°C)

L, W = length and width of trace in mm or mil. Note: L and W must both be in the same units.

t = thickness of trace in mm (1 oz copper = 0.0348mm, 2 oz copper = 0.0696mm)

T = temperature in °C

Example

What is the resistance of a 20 mil long, 5 mil wide trace for a 1 oz Cu thickness at 25°C and 125°C?

Answer

$$R25C = 1.95m\Omega, R125C = 2.72m\Omega$$

$$R = \left(17 \cdot 10^{-6}\Omega \cdot mm\right)\frac{20mil}{(0.0348mm) \cdot 5mil}\left[1 + 3.9 \cdot 10^{-3}/^{\circ}C\left(125^{\circ}C - 25^{\circ}C\right)\right] = 2.72m\Omega \tag{159}$$

PCB trace resistance for 1 oz-Cu

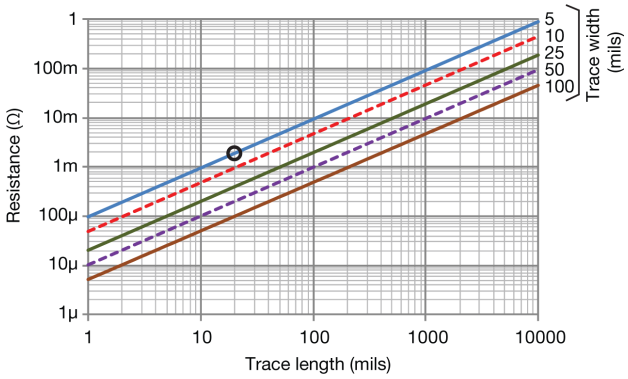


Figure 61. *PCB trace resistance vs. length and width for 1 oz-Cu, 25°C*

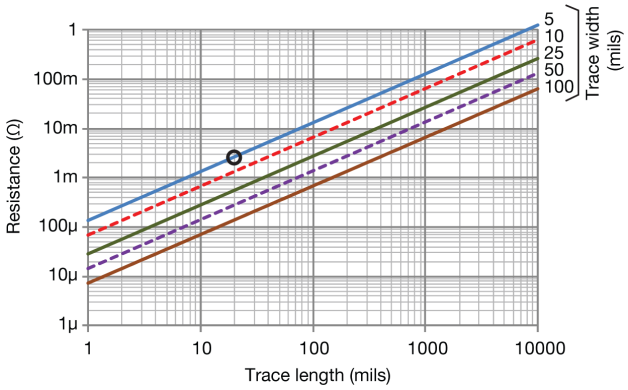


Figure 62. *PCB trace resistance vs. length and width for 1 oz-Cu, 125°C*

Example

What is the resistance of a 20 mil long, 5 mil wide trace for a 1 oz-Cu thickness at 25°C and 125°C?

Answer

R25C = 2 mΩ, R125C = 3 mΩ. The points are circled on the curves.

PCB trace resistance for 2 oz-Cu

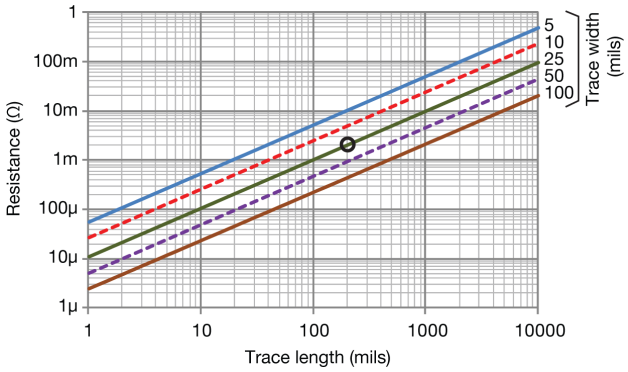


Figure 63. *PCB trace resistance vs. length and width for 2 oz-Cu, 25°C*

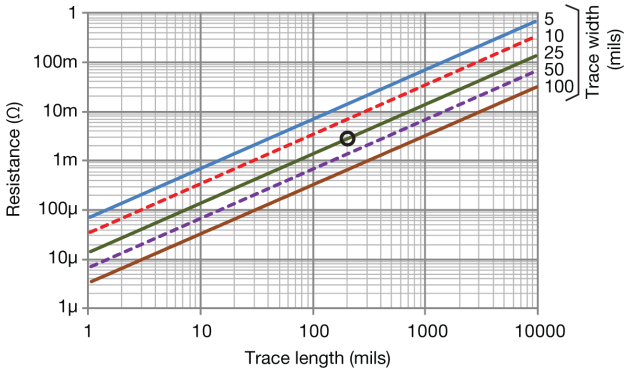


Figure 64. *PCB trace resistance vs. length and width for 2 oz-Cu, 125°C*

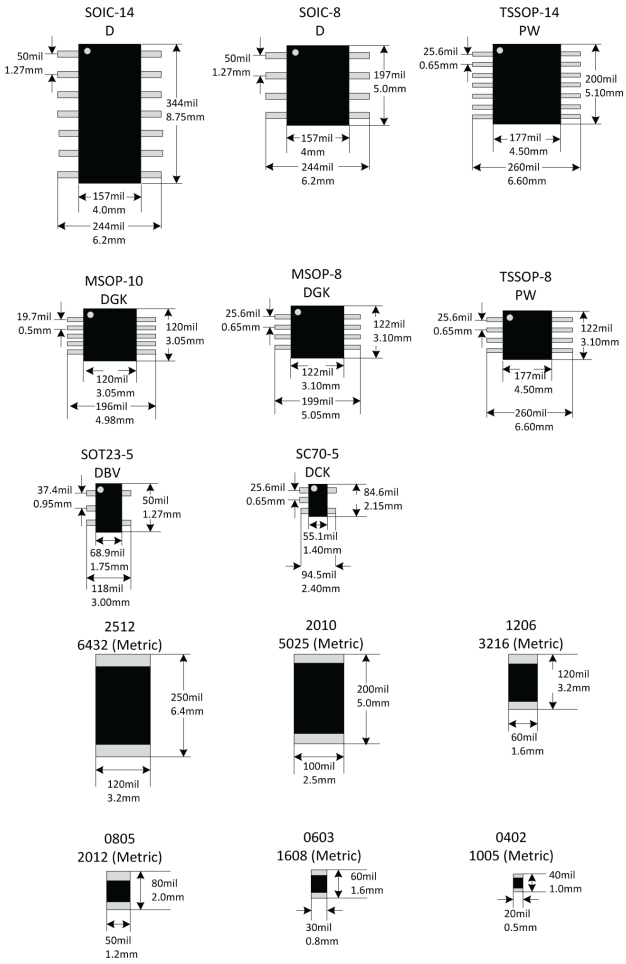
Example

What is the resistance of a 200 mil long, 25 mil wide trace for a 2 oz-Cu thickness at 25°C and 125°C?

Answer

R25C = 2 mΩ, R125C = 3 mΩ. The points are circled on the curves.

Common package type and dimensions



PCB parallel plate capacitance

Capacitance for parallel copper planes

$$C(pF) = \frac{k \cdot l \cdot w \cdot \varepsilon_r}{h} \tag{160}$$

Where

k = permittivity of free space.

Both the metric and imperial version of the constant are given.

k = 8.854 × 10^{-3} pF/mm, or 2.247 × 10^{-4} pF/mil

l = length (metric in mm, or imperial in mil)

w = width (metric in mm, or imperial in mil)

h = separation between planes (metric in mm, or imperial in mil)

ε_r = PCB relative dielectric constant ($\varepsilon_r \approx 4.5$ for FR-4)

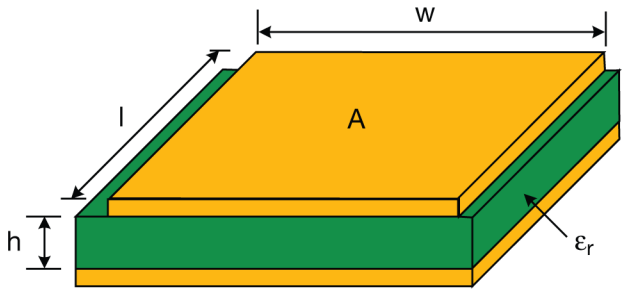


Figure 65. *PCB parallel plate capacitance*

Example

Calculate the total capacitance if l = 5.08mm, w = 12.7mm, h = 1.575mm, and ε_r = 4.5.

Answer

$$C(\text{pF}) = \frac{\left(8.854 \times 10^{-3}\text{pF/mm}\right) \times 5.08\text{mm} \times 12.7\text{mm} \times 4.5}{1.575\text{mm}} = 1.63\text{pF} \tag{161}$$

Example

Calculate the total capacitance if l = 200mil, w = 500mil, h = 62mil, and ε_r = 4.5.

Answer

$$C(\text{pF}) = \frac{\left(2.247 \times 10^{-4}\text{pF/mil}\right) \times 200\text{mil} \times 500\text{mil} \times 4.5}{62\text{mil}} = 1.63\text{pF} \tag{162}$$

PCB microstrip capacitance and inductance

Inductance for microstrip

$$L(\text{nH}) = k_L \cdot l \cdot \ln\left(\frac{5.98 \cdot h}{0.8 \cdot w + t}\right) \tag{163}$$

Capacitance for microstrip

$$C(\text{pF}) = \frac{k_C \cdot l \cdot (\varepsilon_r + 1.41)}{\ln\left(\frac{5.98 \cdot h}{0.8 \cdot w + t}\right)} \tag{164}$$

Characteristic impedance for microstrip

$$Z_O = \sqrt{\frac{L}{C}} = \frac{87\Omega}{\sqrt{(\varepsilon_r + 1.41)}} \cdot \ln\left(\frac{5.98 \cdot h}{0.8 \cdot w + t}\right) \tag{165}$$

Where

k_L = PCB inductance per unit length.

Both the metric and imperial version of the constant are given.

k_L = 2nH/cm, or 5.071nH/in

k_C = PCB capacitance per unit length.

Both the metric and imperial version of the constant are given.

k_C = 0.264pF/cm, or 0.67056pF/in

l = length of microstrip (metric in cm, or imperial in inches)

w = width of microstrip (metric in mm, or imperial in mil)

t = thickness of copper (metric in mm, or imperial in mil)

h = separation between planes (metric in mm, or imperial in mil)

ε_r = PCB dielectric constant ($\varepsilon_r \approx 4.5$ for FR-4)

For imperial: Copper thickness (mils) = 1.37 × (number of ounces)

i.e. 1oz Cu = 1.37mils

i.e. ½oz Cu = 0.684mils

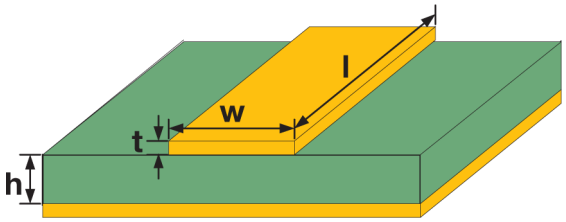


Figure 66. *PCB Microstrip capacitance and inductance*

Example

Calculate the total inductance and capacitance if l = 2.54cm, w = 0.254mm, t = 0.0356mm, h = 0.8mm, and ε_r = 4.5 for FR-4.

Answer

$$\mathrm{L(nH)} = (2\mathrm{nH/cm}) \cdot (2.54\mathrm{cm}) \cdot \ln\left(\frac{5.98 \cdot 0.8\mathrm{mm}}{0.8 \cdot 0.254\mathrm{mm} + 0.0356\mathrm{mm}}\right) = 15.2\mathrm{nH}$$

$$\mathrm{C(pF)} = \frac{(0.264\mathrm{pF/cm}) \cdot (2.54\mathrm{cm}) \cdot (4.5 + 1.41)}{\ln\left(\frac{5.98 \cdot 0.8\mathrm{mm}}{0.8 \cdot 0.254\mathrm{mm} + 0.0356\mathrm{mm}}\right)} = 1.3\mathrm{pF} \tag{166}$$

PCB adjacent copper traces

Same layer

$$C(pF) \approx \frac{k \cdot t \cdot l}{d} \tag{167}$$

Different layers

$$C(pF) \approx \frac{k \cdot \varepsilon_r \cdot w \cdot l}{h} \tag{168}$$

Where

l = length of the copper trace (mil or mm)

k = 8.854×10^{-3}pF/mm, or k=2.247×10^{-4}pF/mil

t = thickness of trace (mil or mm)

d = distance between traces if on same layer (mil or mm)

w = width of trace (mil or mm)

h = separation between planes (mil or mm)

ε_r = PCB dielectric constant ($\varepsilon_r \approx 4.5$ for FR-4)

For imperial: Copper thickness (mils) = 1.37 × (number of ounces)

i.e. 1oz Cu = 1.37mils

i.e. ½oz Cu = 0.684mils

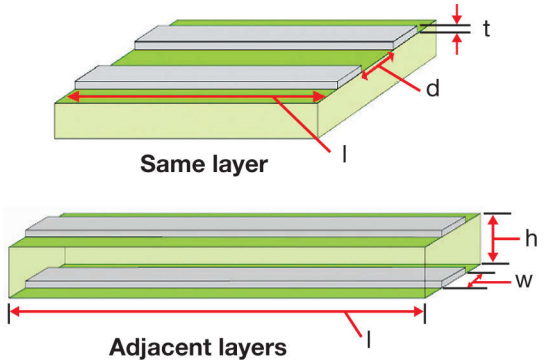


Figure 67. *Capacitance for adjacent copper traces*

Example

Calculate the total capacitance for both cases if l = 2.54mm, t = 0.0348mm, d = 0.254mm, w = 0.635mm, h = 1.6mm, and ε_r = 4.5 for FR-4.

Answer

$$C(\text{pF}) \approx \frac{\left(8.854 \times 10^{-3}\text{pF/mm}\right)(0.0348\text{mm})(2.54\text{mm})}{0.254\text{mm}} = 0.0031\text{pF} \quad \text{(same layer)}$$

$$C(\text{pF}) \approx \frac{\left(8.854 \cdot 10^{-3}\text{pF/mm}\right)(4.5\text{mm})(0.635\text{mm})(2.54\text{mm})}{1.6\text{mm}} = 0.04\text{pF} \quad \text{(adjacent layers)} \tag{16}$$

Example

Calculate the total capacitance for both cases if l = 100mil, t = 1.37mil, d = 10mil, w = 25mil, h = 63mil, and ε_r = 4.5 for FR-4.

Answer

C = 0.0031pF (same layer), C = 0.4pF (adjacent layers). Note: this is the same example as above with imperial units.

PCB via capacitance and inductance

$$L(\text{nH}) \approx k_L \cdot h\left[1 + \ln\left(\frac{4h}{d}\right)\right] \tag{170}$$

Figure 68. *Inductance for via*

$$C(\text{pF}) \approx \frac{k_C \cdot \varepsilon_r \cdot h \cdot d_1}{d_2 - d_1} \tag{171}$$

Figure 69. *Capacitance for via*

Where

k_L = PCB inductance per unit length.

Both the metric and imperial version of the constant are given.

k_L = 0.2nH/mm, or 5.076×10^{-3}nH/mil

k_C = PCB capacitance per unit length.

Both the metric and imperial version of the constant are given.

k_C = 0.0555pF/mm, or 1.41×10^{-3}pF/mil

h = separation between planes

d = diameter of via hole

d_1 = diameter of the pad surrounding the via

d_2 = distance to inner layer ground plane

ε_r = PCB dielectric constant ($\varepsilon_r \approx 4.5$ for FR-4)

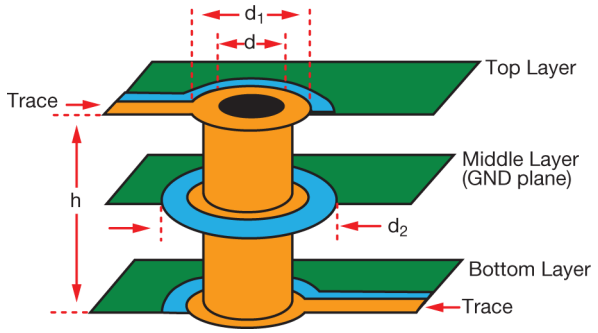


Figure 70. *Inductance and capacitance of via*

Example

Calculate the total inductance and capacitance if h = 1.6mm, d = 0.4mm, d_1 = 0.8mm, and d_2 = 1.5mm.

Answer

$$L(\text{nH}) \approx (0.2\text{nH/mm}) \cdot (1.6\text{mm})\left[1 + \ln\left(\frac{4 \cdot 1.6\text{mm}}{0.4\text{mm}}\right)\right] = 1.2\text{nH}$$

$$C(\text{pF}) \approx \frac{(0.0555\text{pF/mm}) \cdot (4.5) \cdot (1.6\text{mm}) \cdot (0.8\text{mm})}{1.5\text{mm} - 0.8\text{mm}} = 0.46\text{pF} \quad (172)$$

Example

Calculate the total inductance and capacitance if h = 63mil, d = 15.8mil, d_1 = 31.5mil, and d_2 = 59mil.

Answer

L = 1.2nH, C = 0.46pF. Note: this is the same example as above with imperial units.

Table 20. Coaxial cable information

Type	Z_O	Capacitance / length (pF/feet)	Outside diameter (inches)	dB attenuation /100 ft at 750 MHz	Dielectric type	Application
RG-58	53.5Ω	28.8	0.195	13.1	PE	Test equipment and RF power to a few hundred watts, and a couple hundred MHz
RG-8	52Ω	29.6	0.405	5.96	PE	RF power to a few kW, up to several hundred MHz
RG-214/U	50Ω	30.8	0.425	6.7	PE	
9914	50Ω	26.0	0.405	4.0	PE	
RG-6	75Ω	20	0.270	5.6	PF	Video and CATV applications. RF to a few hundred watts, up to a few hundred MHz, sometimes to higher frequencies if losses can be tolerated.
RG-59/U	73Ω	29	0.242	9.7	PE	
RG-11/U	75Ω	17	0.412	3.65	PE	RF power to a few kW, up to several hundred MHz
RG-62/U	93Ω	13.5	0.242	7.1	ASP	Used in some test equipment and 100Ω video applications
RG-174	50Ω	31	0.100	23.5	PE	Miniature coax used primarily for test equipment interconnection. Usually short runs due to higher loss.
RG-178/U	50Ω	29	0.071	42.7	ST	

Coaxial cable equations

$$\frac{C}{l} = \frac{2\pi\varepsilon}{\ln\left(\frac{D}{d}\right)} \tag{173}$$

Figure 71. *Capacitance per length*

$$\frac{L}{l} = \frac{\mu}{2\pi}\ln\left(\frac{D}{d}\right) \tag{174}$$

Figure 72. *Inductance per length*

$$Z_o = \sqrt{\frac{L}{C}} = \frac{1}{2\pi}\cdot\sqrt{\frac{\mu}{\varepsilon}}\cdot\ln\left(\frac{D}{d}\right) \tag{175}$$

Figure 73. *Characteristic impedance*

Where

L = inductance in henries (H)

C = capacitance in farads (F)

Z = impedance in ohms (Ω)

d = diameter of inner conductor

D = inside diameter of shield, or diameter of dielectric insulator

ε = dielectric constant of insulator ($\varepsilon = \varepsilon_r\ \varepsilon_o$)

μ = magnetic permeability ($\mu = \mu_r\ \mu_o$)

l = length of the cable

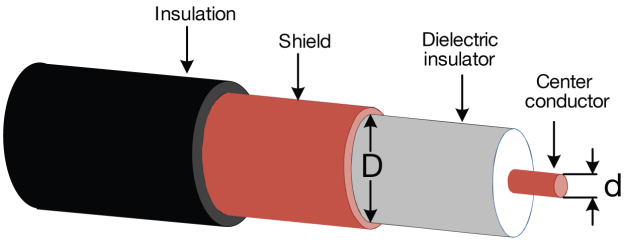


Figure 74. *Coaxial cable cutaway*

Table 21. Resistance per length for different wire types (AWG)

AWG	Stds	Outside diameter		Area		DC resistance	
		in	mm	circular mils	mm^2	Ω / 1000 ft	Ω / km
36	Solid	0.005	0.127	25	0.013	445	1460
36	7/44	0.006	0.152	28	0.014	371	1271
34	Solid	0.0063	0.160	39.7	0.020	280	918
34	7/42	0.0075	0.192	43.8	0.022	237	777
32	Solid	0.008	0.203	67.3	0.032	174	571
32	7/40	0.008	0.203	67.3	0.034	164	538
30	Solid	0.010	0.254	100	0.051	113	365

Table 21. Resistance per length for different wire types (AWG) (continued)

AWG	Stds	Outside diameter		Area		DC resistance	
		in	mm	circular mils	mm^2	Ω / 1000 ft	Ω / km
30	7/38	0.012	0.305	112	0.057	103	339
28	Solid	0.013	0.330	159	0.080	70.8	232
28	7/36	0.015	0.381	175	0.090	64.9	213
26	Solid	0.016	0.409	256	0.128	43.6	143
26	10/36	0.021	0.533	250	0.128	41.5	137
24	Solid	0.020	0.511	404	0.205	27.3	89.4
24	7/32	0.024	0.610	448	0.229	23.3	76.4
22	Solid	0.025	0.643	640	0.324	16.8	55.3
22	7/30	0.030	0.762	700	0.357	14.7	48.4
20	Solid	0.032	0.813	1020	0.519	10.5	34.6
20	7/28	0.038	0.965	1111	0.562	10.3	33.8
18	Solid	0.040	1.020	1620	0.823	6.6	21.8
18	7/26	0.048	1.219	1770	0.902	5.9	19.2
16	Solid	0.051	1.290	2580	1.310	4.2	13.7
16	7/24	0.060	1.524	2828	1.442	3.7	12.0
14	Solid	0.064	1.630	4110	2.080	2.6	8.6
14	7/22	0.073	1.854	4480	2.285	2.3	7.6

Table 22. Maximum current vs. AWG

Wire gauge	Polyethylene Neoprene Polyvinylchloride (semi-ridged) at 80°C	Polypropylene Polyethylene (high density) at 90°C	Polyvinylchloride Nylon at 105°C	Kynar Polyethylene Thermoplastic at 125°C	Kapton Teflon Silicone at 200°C
AWG	I_{max} (A)	I_{max} (A)	I_{max} (A)	I_{max} (A)	I_{max} (A)
30	2	3	3	3	4
28	3	4	4	5	6
26	4	5	5	6	7
24	6	7	7	8	10
22	8	9	10	11	13
20	10	12	13	14	17
18	15	17	18	20	24
16	19	22	24	26	32
14	27	30	33	40	45
12	36	40	45	50	55
10	47	55	58	70	75

Note

The table shows the current required to raise the temperature of a single insulated conductor in free air (30°C ambient) to the limits of various insulation types.

Example

What is the maximum current that can be applied to a 30 gauge Teflon wire in a room temperature environment?

What will the self-heating be?

Answer

I_{max} = 4A

Wire temperature = 200°C

Notes

Sensor

- Thermistor
- Resistive temperature detector (RTD)
- Diode equation vs. temperature
- Thermocouple (J and K)
- Notes

Thermistor

Table 23. Temperature sensor overview

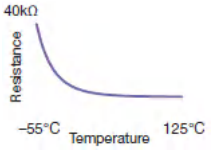
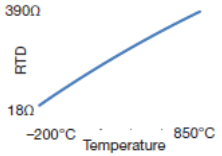
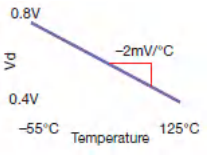
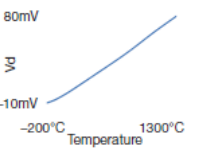
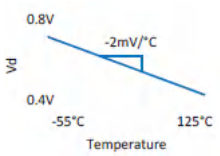
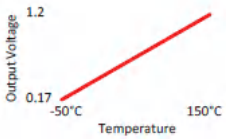
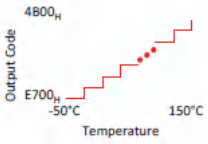
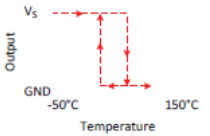
	Thermistor	RTD	Diode	Thermocouple
				
Temp range	–55°C< T < 150°C	–200°C< T < 850°C	–55°C< T < 150°C	–250°C< T < 1800°C
Cost	Very low	High	Low	Low
Accuracy	Good accuracy at one temperature Less accurate over full range	Excellent accuracy	Poor accuracy without calibration	Goodaccuracy with polynomial correction
Linearity	Verynonlinear. Follows reciprocal of logarithmic function	Fairlylinear Nonlinearity < 4.5% of full scale Relatively simple quadratic function	Fairly linear slope ≈ –2mV/CSlope varies according to current excitation, diode type, and diode processing	Fairlylinear Nonlinearity < 10% of full scale Complex 10th order polynomial
Construction	Less rugged	Dependson type (can be rugged)	Rugged	Most rugged
Output range	Typically 10s to 100s of kΩ fullscale Very wide variation in resistance	18 to 390Ω for PT100 180 to 3.9kΩ for PT1000	0.4to 0.8V	10sof millivolts
Applications	General purpose	Scientific and industrial	Low cost temperature monitor Low cost linear response	Industrial temperature measurement
General	Requires excitation	Requires excitation	Requires excitation	Self-powered Requires cold junction comp

Table 24. IC temperature sensor overview

	Diode	Analog IC temperature sensor	Digital IC temperature sensor	Temperature switch/thermostat
				
Temp range	–55°C< T < 150°C	–55°C< T < 150°C	–55°C< T < 150°C	–55°C< T < 150°C
Cost	Very low	Low	Low	Low
Accuracy	Poor accuracy without calibration	Gooddevice accuracy without calibration. Total T_{error} ≤ 0.13°C.	Zero calibration required. Total T_{error} including ADC ≤ 0.1°C.	Zero calibration required. Total T_{error} including comparator ≤0.1°C.
Linearity	Fairly linear ≈ -2mV/°C. Slope varies according to current excitation, diode type,and diode processing from -5.5mV/C to +19.5mV/C.	Fairlylinear. With analog sensors a variety of slope options in the range from -5.5mV/C to +19.5mV/C.	Directreadout of temperature value. 8 to 16 bits of resolution.	Programmable temperature threshold
Construction	Rugged	Rugged	Rugged	Rugged
Output range	0.4Vto 0.8V	0 to 3V for analog. Different output ranges for different devices.	Digital interfaces: I2C, SPI, UART	Active high or active low output
Applications	Low cost temperature monitor. Low cost linear response.	General purpose, industrial and automotive	General purpose, industrial and automotive	General purpose, industrial and automotive
General	Requires excitation	No external excitation required. Analog output normally directly connected to ADC.	Integrated temperature sensorand ADC/comparator. Options to measure remote diodes.	Resistorprogrammable, pin programmable, factory preset

Resistive temperature detector (RTD)

RTD equation temperature to resistance (T≥0°C and T<0°C)

RTD resistance for T<0°C

$$R_{RTD} = R_0\left[1 + A_0T + B_0T^2 + C_0(T - 100)T^3\right] \quad (176)$$

RTD resistance for T≥0°C

$$R_{RTD} = R_0\left[1 + A_0T + B_0T^2\right] \quad (177)$$

Where

R_{RTD} = resistance of RTD over temperature range of (–200°C < T < 850°C)

R_0 = 100Ω for PT-100, 1000Ω for PT-1000

A_0, B_0, C_0 = Callendar-Van Dusen coefficients

T = temperature in degrees Celsius (°C)

RTD equation resistance to temperature (T≥0°C or R_{RTD} ≥ R_0)

Temperature for T≥0°C or R_{RTD} ≥ R_0

$$T = \frac{-A_0 + \sqrt{A_0^2 - 4B_0\left(1 - \frac{R_{RTD}}{R_0}\right)}}{2B_0} \quad (178)$$

Where

R_{RTD} = resistance of RTD over temperature range of (T≥0°C)

R_0 = 100Ω for PT-100, 1000Ω for PT-1000

A_0, B_0, C_0 = Callendar-Van Dusen coefficients

T = temperature in degrees Celsius (°C)

Table 25. Callendar-Van Dusen coefficients for different RTD standards

	IEC-751 DIN 43760 BS 1904 ASTM-E1137 EN-60751	JISC 1604	US Industrial Standard D-100 American	US Industrial Standard American	ITS-90
A_0	+3.9083E-3	+3.9739E-3	+3.9787E-3	+3.9692E-3	+3.9888E-3
B_0	–5.775E-7	–5.870E-7	–5.8686E-7	–5.8495E-7	–5.915E-7
C_0	–4.183E-12	–4.4E-12	–4.167E-12	–4.233E-12	–3.85E-12

Example

What is the temperature given an ITS-90 PT100 resistance of 120Ω?

Answer

$$T = \frac{-\left(3.9888 \cdot 10^{-3}\right) + \sqrt{\left(3.9888 \cdot 10^{-3}\right)^2 - 4\left(-5.915 \cdot 10^{-7}\right)\left(1 - \frac{120}{100}\right)}}{2\left(-5.915 \cdot 10^{-7}\right)} = 50.5^{\circ}C \quad (179)$$

RTD equation resistance to temperature (T< 0°C or R_{RTD} < R_0)

Temperature for T<0°C or R_{RTD} < R_0

$$T = \sum_{i=0}^{n} \alpha_i (R_{RTD})^i \quad (180)$$

Where

T = temperature in degrees Celsius (°C)

R_{RTD} = resistance of RTD over temperature range of (T<0°C)

α_i = polynomial coefficients for converting RTD resistance to temperature for T<0°C

Table 26. Coefficients for 5th order RTD resistance to temperature

	IEC-751 DIN 43760 BS 1904 ASTM-E1137 EN-60751	JISC 1604	US Industrial Standard D-100 American	US Industrial Standard American	ITS-90
α_0	-2.420199E+02	-2.381987E+02	-2.381832E+02	-2.386381E+02	-2.379147E+02
α_1	2.222812E+00	2.189835E+00	2.195550E+00	2.197285E+00	2.201058E+00
α_2	2.585894E-03	2.522738E-03	2.441461E-03	2.480324E-03	2.322506E-03
α_3	-4.825976E-06	-4.781625E-06	-4.751529E-06	-4.778784E-06	-4.628394E-06
α_4	-2.818583E-08	-2.704445E-08	-2.385758E-08	-2.518695E-08	-1.971986E-08
α_5	1.524399E-10	1.473912E-10	1.350936E-10	1.403820E-10	1.184331E-10

Example

Find the temperature given an ITS-90 PT100 resistance of 60 Ω.

Answer

R=60

$$T = (-2.379147E+02) + (2.201058E+00) \times R + (2.322506E-03) \times R^2 + (-4.628394E-06) \times R^3 + (-1.971986E-08) \times R^4 + (1.184331E-10) \times R^5 = -98.653 \quad (181)$$

Diode equation vs. temperature

Diode voltage

$$V_D = \frac{nkT}{q}\ln\left(\frac{1}{I_S} + 1\right) \approx \frac{nkT}{q}\ln\left(\frac{1}{I_S}\right) \quad (182)$$

Where

V_D = diode voltage vs. temperature and current

n = diode ideality factor (ranges from 1 to 2)

k = 1.38 × 10^{-23} J/K, Boltzmann's constant

T = temperature in Kelvin

q = 1.60 × 10^{-19} C, charge of an electron

I = forward diode current in amps

I_S = saturation current

Saturation current

$$I_S = \alpha T^{(3/n)}\exp\left(-\frac{qV_G}{nkT}\right) \quad (183)$$

Where

I_S = saturation current

α = constant related to the cross sectional area of the junction

V_G = diode voltage vs. temperature and current

n = diode ideality factor (ranges from 1 to 2)

k = 1.38 × 10^{-23} J/K, Boltzmann's constant

T = temperature in Kelvin

q = 1.60 × 10^{-19} C, charge of an electron

Diode voltage versus temperature

Figure 75 shows an example of the temperature drift for a diode. Depending on the characteristics of the diode and the forward current the slope and offset of this curve will change. However, typical diode drift is about –2mV/°C. A forward drop of about 0.6V is typical for room temperature.

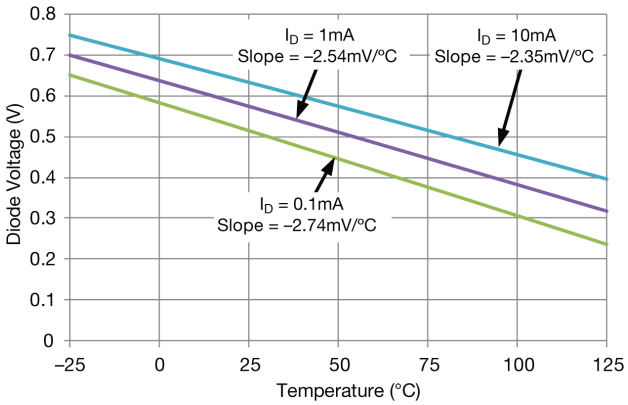


Figure 75. *Diode voltage drop vs. temperature*

Thermocouple (J and K)

Type J thermocouples translating temperature to voltage (ITS-90 standard)

Thermoelectric voltage

$$V_T = \sum_{i=0}^{n} c_i(T)^i \tag{184}$$

Where

V_T = thermoelectric voltage

T = temperature in degrees Celsius

c_i = translation coefficients

Table 27. Type J thermocouple temperature to voltage coefficients

Type J thermocouple temperature to voltage		
Temperature	**–219°C to 760°C**	**760°C to 1,200°C**
c_0	0.0000000000E+00	2.9645625681E+05
c_1	5.0381187815E+01	–1.4976127786E+03
c_2	3.0475836930E-02	3.1787103924E+00
c_3	–8.5681065720E-05	–3.1847686701E-03
c_4	1.3228195295E-07	1.5720819004E-06
c_5	–1.7052958337E-10	–3.0691369056E-10
c_6	2.0948090697E-13	—
c_7	–1.2538395336E-16	—
c_8	1.5631725697E-20	—

Type J thermocouples translating voltage to temperature (ITS-90 standard)

Temperature

$$T = \sum_{i=0}^{n} c_i(V_t)^i \tag{185}$$

Table 28. Type J thermocouple voltage to temperature coefficients

Type J thermocouple voltage to temperature			
Temperature	**–219°C to 0°C**	**0°C to 760°C**	**760°C to 1,200°C**
Voltage	-8.095mV to 0V	0V to 42.919mV	42.919mV to 69.553mV
c_0	0.000000000E+00	0.000000000E+00	–3.113581870E+03
c_1	1.952826800E-02	1.978425000E-02	3.005436840E-01
c_2	–1.228618500E-06	–2.001204000E-07	–9.947732300E-06
c_3	–1.075217800E-09	1.036969000E-11	1.702766300E-10
c_4	–5.908693300E-13	–2.549687000E-16	–1.430334680E-15
c_5	–1.725671300E-16	3.585153000E-21	4.738860840E-21
c_6	–2.813151300E-20	–5.344285000E-26	—
c_7	–2.396337000E-24	5.099890000E-31	—
c_8	–8.382332100E-29	—	—

Type K thermocouples translating temperature to voltage (ITS-90 standard)

Thermoelectric voltage for T<0°C

$$V_T = \sum_{i=0}^{n} c_i (T)^i \tag{186}$$

Thermoelectric voltage for T>0°C

$$V_T = \left[\sum_{i=0}^{n} c_i (T)^i \right] + \alpha_0 e^{\left[\alpha_1 (T - 126.9686)\right]^2} \tag{187}$$

Where

V_T = thermoelectric voltage, T = temperature in degrees Celsius, c_i = translation coefficients, α_0, α_1 = translation coefficients

Table 29. Type K thermocouple temperature to voltage coefficients

Temperature	**–270°C to 0°C**	**0°C to 1,372°C**
c_0	0.0000000000E+00	–1.7600413686E+01
c_1	3.9450128025E+01	3.8921204975E+01
c_2	2.3622373598E-02	1.8558770032E-02
c_3	–3.2858906784E-04	–9.9457592874E-05
c_4	–4.9904828777E-06	3.1840945719E-07
c_5	–6.7509059173E-08	–5.6072844889E-10
c_6	–5.7410327428E-10	5.6075059059E-13
c_7	–3.1088872894E-12	–3.2020720003E-16
c_8	–1.0451609365E-14	9.7151147152E-20
c_9	–1.9889266878E-17	–1.2104721275E-23
c_{10}	–1.6322697486E-20	—
α_0	—	1.1859760000E+02
α_1	—	–1.1834320000E-04

Type K thermocouples translating voltage to temperature (ITS-90 standard)

Temperature

$$T = \sum_{i=0}^{n} C_i (V_t)^i \quad (188)$$

Table 30. Type K thermocouple voltage to temperature coefficients

Temperature	-200°C to 0°C	0°C to 500°C	500°C to 1,372°C
Voltage	-5.891mV to 0V	0V to 20.644mV	20.644mV to 54.886mV
c_0	0.0000000E+00	0.0000000E+00	–1.3180580E+02
c_1	2.5173462E-02	2.5083550E-02	4.8302220E-02
c_2	–1.1662878E-06	7.8601060E-08	–1.6460310E-06
c_3	–1.0833638E-09	–2.5031310E-10	5.4647310E-11
c_4	–8.9773540E-13	8.3152700E-14	–9.6507150E-16
c_5	–3.7342377E-16	–1.2280340E-17	8.8021930E-21
c_6	–8.6632643E-20	9.8040360E-22	–3.1108100E-26
c_7	–1.0450598E-23	–4.4130300E-26	—
c_8	–5.1920577E-28	1.0577340E-30	—
c_9	—	–1.0527550E-35	—

Table 31. Seebeck coefficients for different material

Material	Seebeck coefficient	Material	Seebeck coefficient	Material	Seebeck coefficient
Aluminum	4	Gold	6.5	Rhodium	6
Antimony	47	Iron	19	Selenium	900
Bismuth	–72	Lead	4	Silicon	440
Cadmium	7.5	Mercury	0.6	Silver	6.5
Carbon	3	Nichrome	25	Sodium	–2.0
Constantan	–35	Nickel	–15	Tantalum	4.5
Copper	6.5	Platinum	0	Tellurium	500
Germanium	300	Potassium	–9.0	Tungsten	7.5

Note

Units are µV/°C. All data at temperature of 0°C.

Thermistor: Resistance to temperature, Steinhart-Hart equation

Convert resistance to temperature for a thermistor

$$\frac{1}{T} = a + b\ln(R) + c[\ln(R)]^3 \quad (189)$$

Where

T = temperature in Kelvin

a, b, c = Steinhart-Hart equation constants

R = resistance in ohms

Thermistor: Temperature to resistance, Steinhart-Hart equation

Convert temperature to resistance for a thermistor

$$R = \exp\left[\left(y-\frac{x}{2}\right)^{\frac{1}{3}} - \left(y+\frac{x}{2}\right)^{\frac{1}{3}}\right] \tag{190}$$

Factor used in Equation 165

$$x = \frac{a-\frac{1}{T}}{c} \tag{191}$$

Factor used in Equation 165

$$y = \sqrt{\left(\frac{b}{3\,c}\right)^3 + \frac{x^2}{4}} \tag{192}$$

Where

R = resistance in Ω

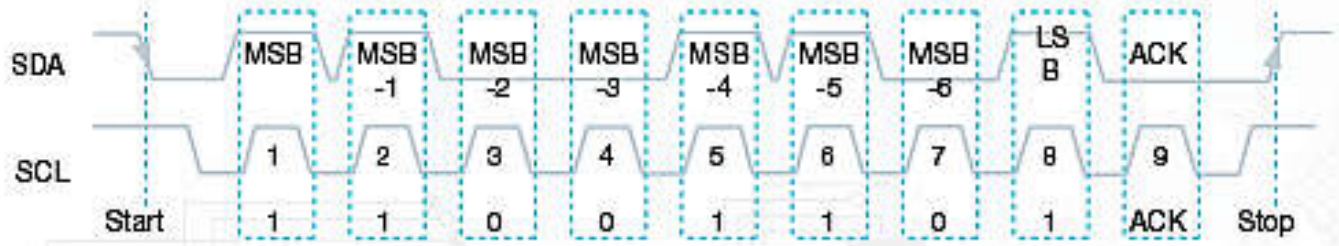
T = temperature in Kelvin

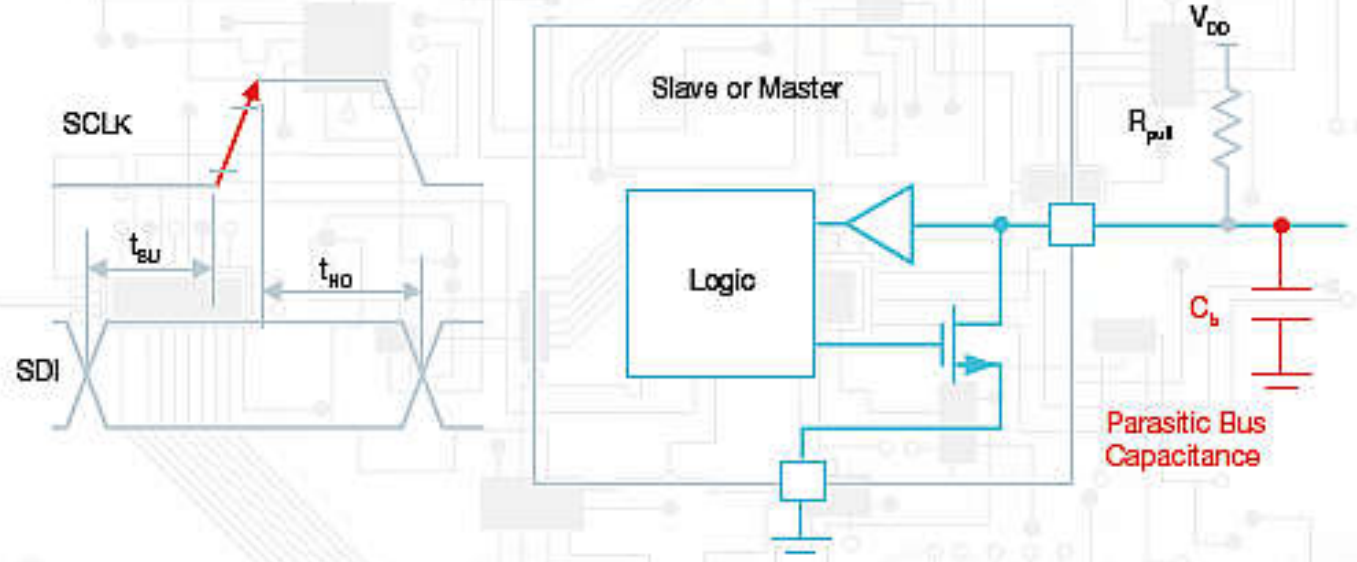
a, b, c = Steinhart-Hart equation constants

x, y = Steinhart-Hart factors used in temperature to resistance equation

Notes

Digital



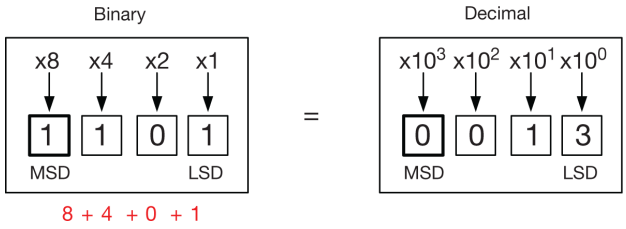


Binary/hex conversions

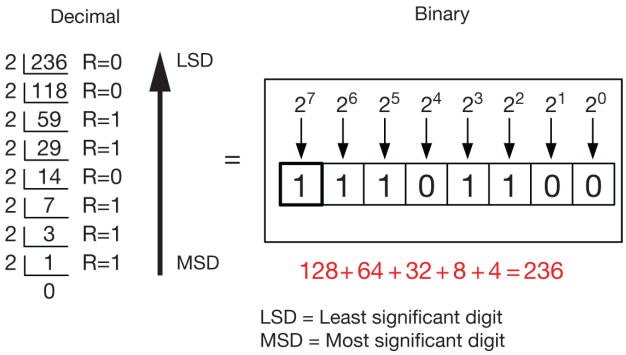
Numbering systems: Binary, decimal, and hexadecimal

Binary (Base-2)	0					1									
Decimal (Base-10)	0	1	2	3	4	5	6	7	8	9					
Hexadecimal (Base-16)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Example conversion: Binary to decimal

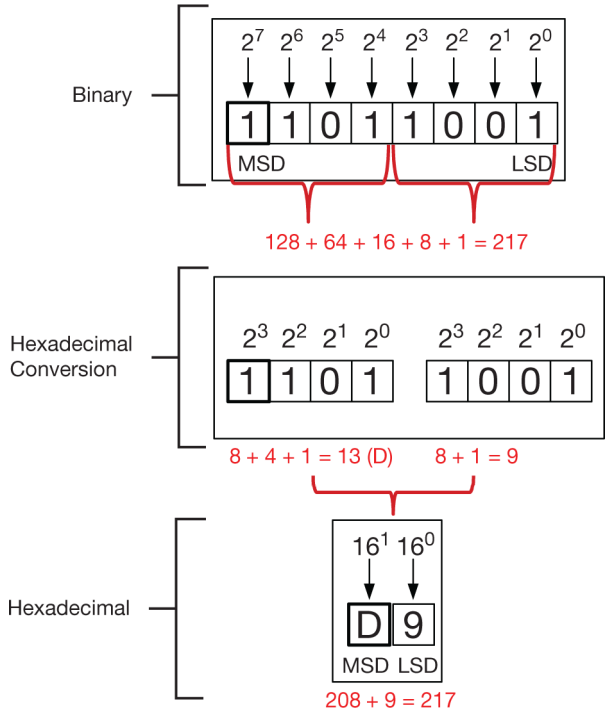


Example conversion: Decimal to binary



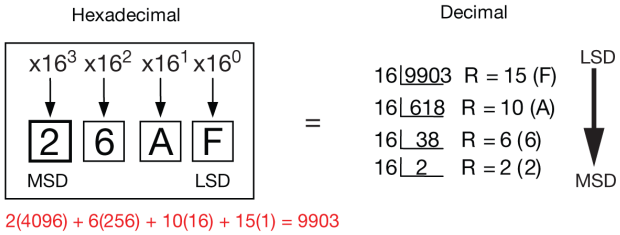
LSD = Least significant digit
MSD = Most significant digit

Example conversion: Binary to hexadecimal



Example conversion: Hexadecimal to decimal and decimal to hexadecimal

Decimal (Base-10)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexadecimal (Base-16)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F



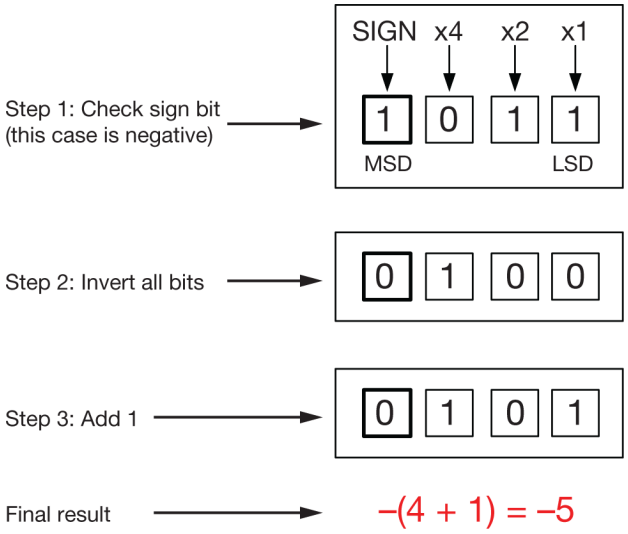
LSD = Least significant digit
MSD = Most significant digit

Data formats

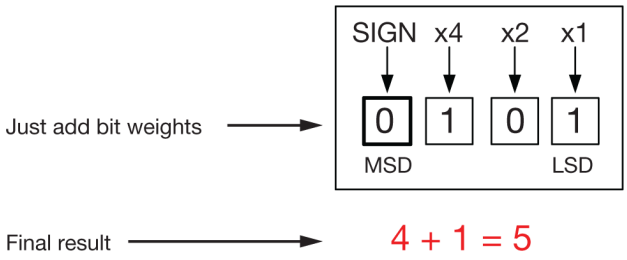
Table 32. Different data formats

Code	Straight binary	Offset binary	2's complement
Binary	Decimal value	Decimal value	Decimal value
11111111	255	127	–1
11000000	192	64	–64
10000000	128	0	–128
01111111	127	–1	127
01000000	64	–64	64
00000000	0	–128	0

Converting two's complement to decimal: Negative number example



Converting two's complement to decimal: Positive number example



Digital logic thresholds

Input logic thresholds = the voltage range a logic device will sense a logic high or low as specified in the data sheet. Applying an input voltage outside of this range to the device will have unpredictable results.

Output logic thresholds = the output voltage range of a logic device driving a logic high or low as specified in the data sheet. The output level range is normally specified with current loads (sourcing for logic high and sinking for logic low).

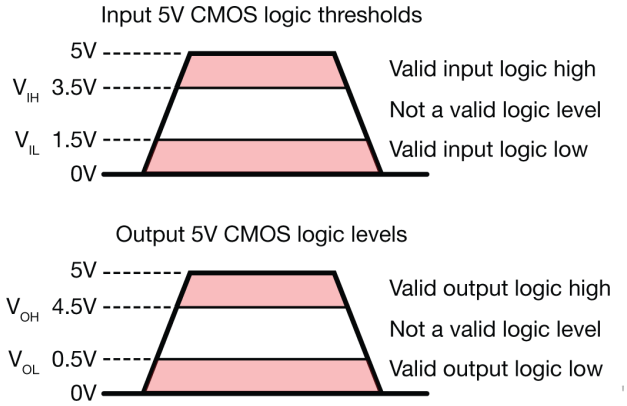


Figure 76. *Valid input logic levels for 5V CMOS*

Table 33. CMOS logic thresholds

	5V CMOS		3.3V CMOS		2.5V CMOS	1.8V CMOS
V_{CC}	5.0		3.3		2.5	1.8
V_{OH}	4.5	0.9· VCC	2.97	0.9· VCC	2.0	1.35
V_{IH}	3.5	0.7· VCC	2.31	0.7· VCC	1.7	1.17
V_{IL}	1.5	0.3· VCC	0.99	0.3· VCC	0.7	0.63
V_{OL}	0.5	0.1· VCC	0.33	0.1· VCC	0.4	0.45
GND	0.0		0.0		0.0	0.0

Table 34. TTL logic thresholds

	5V TTL	3.3V LVTTL
V_{CC}	5.0	3.3
V_{OH}	2.4	2.4
V_{IH}	2.0	1.5
V_{IL}	0.8	0.8
V_{OL}	0.4	0.4
GND	0.0	0.0

Where

V_{CC} and GND = supply voltage and ground for the device

V_{OH} = minimum output logic high level

V_{IH} = minimum input high logic level

V_{IL} = maximum input logic low level

V_{OL} = maximum output logic low level

Serial peripheral interface

SPI bus (Serial Peripheral Interface) hardware overview

- In SPI interfaces the master can connect to one or more slave devices
- In cases when multiple slave devices are used, the master will use multiple chip select ($\overline{CS}$) lines

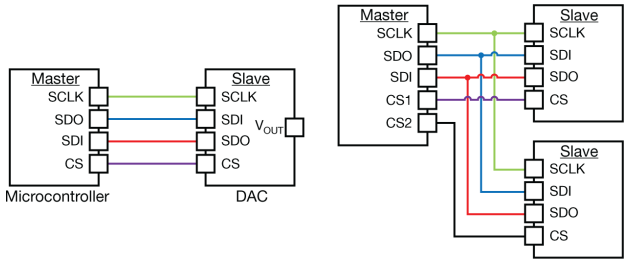


Figure 77. *SPI master and slave configurations*

Data and control lines

$\overline{CS}$ (chip select) = sometimes referred to as slave select. $\overline{CS}$ is driven by the master and arbitrates over the SPI bus. When driven low, the SPI bus is active.

SDO/SDI (serial data in and serial data out) = these names describe data flow for the device. The system names describe the data flow relationship between the master and slave. System names: MOSI = Master Out Slave In and MISO = Master In Slave Out. Example: SDO on a slave is MISO in the system and SDI is MOSI in the system.

SCLK (serial clock) = this is a square wave driven by the SPI master. Data on SDO and SDI have relative timing to the SCLK signal which controls the latching of the data on the SPI bus.

SPI data latching

- SPI data is latched on the rising or falling edge of SCLK
- The edge data is latched on is called the critical edge
- The figure below illustrates latching logic 1 on rising edge and logic 0 on falling edge

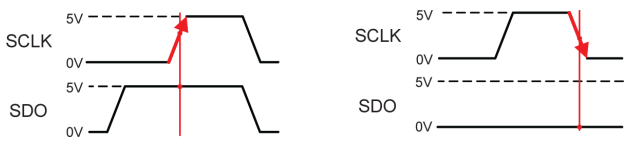


Figure 78. *SPI SCLK critical edge*

SPI read sequence example

1. Critical edge is rising edge
2. Master output writing to slave (SDI label relative to slave device)
3. The active low $\overline{CS}$ pin is driven low to 0V, activating the slave SPI bus 4. Data is clocked in from MSB to LSB on the rising edge of SCLK
4. Completed SPI transaction data is binary 1011001

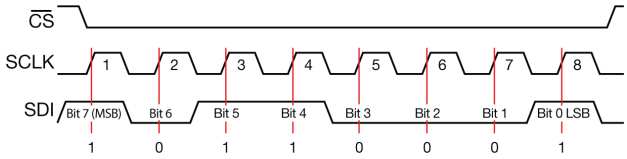


Figure 79. *Example SPI write sequence*

SPI critical edge

t_{SU} (setup time) = defines how long before the critical edge that the data on SDI must already be set and settled

t_{HO} (hold time) = defines how long after the critical edge data must be maintained on SDI.

t_{DO} (delay time) - defines the delay before data is valid after the critical edge for SDO.

Violation of any timing requirement could result in corruption of data.

The timing parameters, t_{SU}, t_{HO} and t_{DO}, are defined relative to the critical edge. In the example below for SDI the rising edge of SCLK is the critical edge and for SDO the falling edge of SCLK is the critical edge.

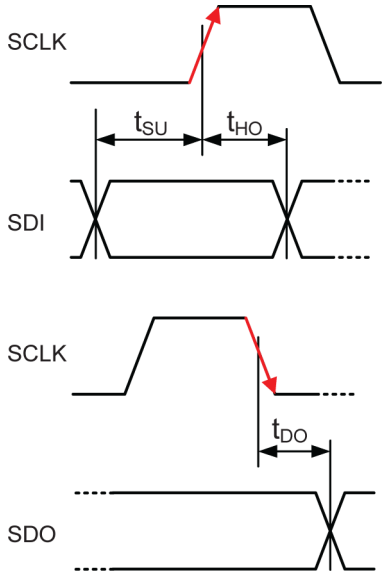


Figure 80. *Setup and hold timing illustration*

SPI modes

CPHA (clock phase) = defines which edge data is latched on, a 0 representing the first edge and a 1 representing the second edge

CPOL (clock polarity) = defines whether the clock idles high or low in between SPI frames. CPOL = 0 idles low, CPOL = 1 idles high.

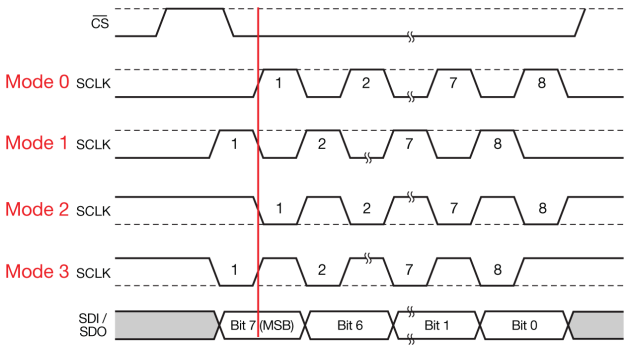


Figure 81. *SPI modes of operation*

Mode	CPOL	CPHA	Critical edge	Clock phase
0	0	0	Rising edge	Idles low
1	0	1	Falling edge	Idles low
2	1	0	Rising edge	Idles high
3	1	1	Falling edge	Idles high

Inter-integrated circuit (I2C) bus

I²C bus (Inter-Integrated Circuit) hardware overview

- On I²C buses the master can connect to one or more slave devices
- The slave is selected by its I2C address. This allows one controller to connect to many slaves on the two-wire bus.

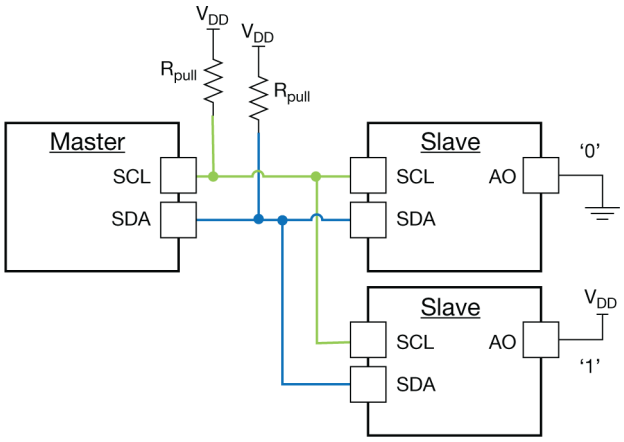


Figure 82. *I²C master and slave hardware connections*

Data and control lines

SCL (serial clock) = this is a square wave driven by the master that controls how fast data is sent and when data is latched to the slave device(s)

SDA (serial data) = both master and slave place data on this line in sync with the clock pulses in a half-duplex fashion. Data on this line includes address, control, and communication data.

I²C addressing

- Typical addressing in I²C is 7-bit addressing with an additional bit for read or write indication
- Each device on the I²C bus must have a unique address
- Duplicate addresses will result in communication errors
- Some devices may have pin programmable I²C addresses

Address byte

MSB						LSB	R/$\overline{W}$
1	0	0	1	1	0	A0	1/0

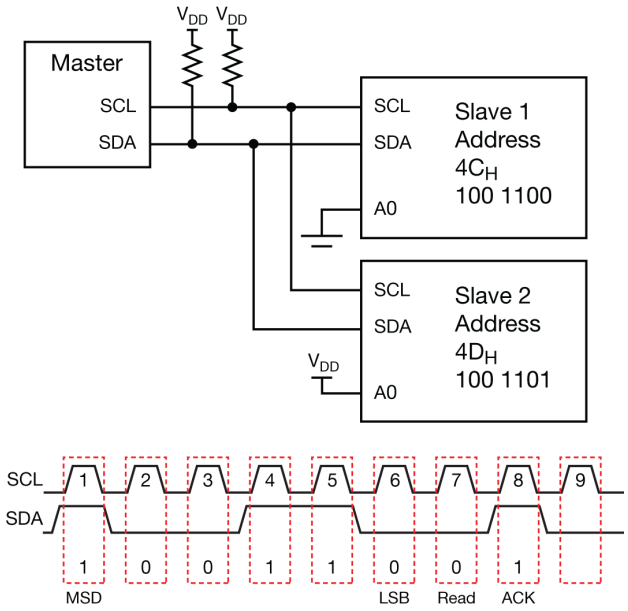


Figure 83. *I²C addressing*

I²C communication

START = initiated by the master pulling SDA low while SCL is high

STOP = initiated by the master releasing the SDA pin high while SCL is high

ACK (acknowledge) = each transfer in I²C is a single byte or 8-bits, with one SCL pulse per bit. The 9th pulse in each exchange is reserved for an acknowledgement signal from the slave, or an ACK signal. The ACK signal indicates that the previous transfer was successful.

Example I²C write sequence:

1. The master pulls down SDA to generate a START condition
2. The first bit is set up and the master pulls down and releases SCL to clock data into the DAC

3. On the 9th bit the master does not pull down SDA. If the slave pulls down SDA the 8-bit transaction is acknowledged.
4. The completed transaction in binary is 11001101

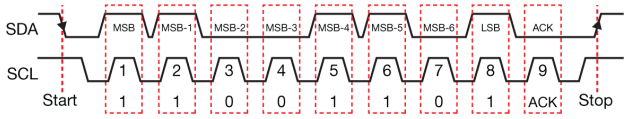


Figure 84. *Complete I²C transaction*

For valid data transfer:

- SDA must remain stable the entire time that SCL is high for a bit transfer to be valid
- SDA is only allowed to transition in between SCL pulses when SCL is low
- Instances where SDA changes while SCL is high are interpreted as START, RESTART, or STOP conditions

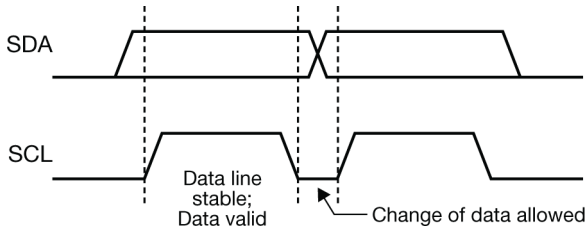


Figure 85. *I²C data transfer*

I²C interface circuitry and rise/fall timing

The figure below illustrates the internal structure for an I²C SCL or SDA pin. The transistor will turn on for logic low discharging C_b to logic low. The transistor will turn off for a logic high and the pull-up, R_{pull}, will charge C_b to a logic high.

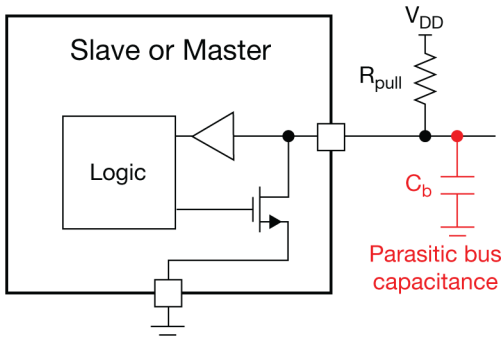


Figure 86. *I²C data transfer*

t_r (rise time) = the maximum amount of time for the signal to transition from logic low to logic high. Since I²C data is an open drain signal, rise time is set by the RC time constant of the pull-up resistance and the bus capacitance.

t_f (fall time) = the maximum amount of time for the signal to transition from logic high to logic low

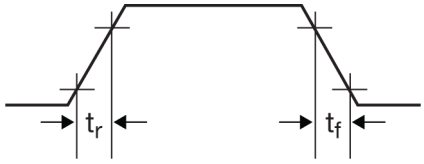


Figure 87. *I²C rise and fall timing*

I²C pull-up resistor selection

Minimum I²C pull-up resistance

$$R_{Pull(Min)} = \frac{(V_{DD} - V_{OLMAX})}{I_{SinkMax}} \quad (193)$$

Maximun I²C pull-up resistance

$$R_{Pull(Max)} = \frac{t_r}{(0.8473 \times C_b)} \quad (194)$$

Where

$R_{Pull(Min)}$ = this is the minimum pull-up resistance. This will give the shortest rise time. Using a pull-up smaller than this will draw too much current when the output transistor is on (logic low) and violate the maximum logic low output specification.

$R_{Pull(Max)}$ = maximum pull-up resistance. This will give the longest rise time. Using a pull-up resistance larger than this will violate timing requirements.

V_{DD} = supply voltage

V_{OLMAX} = maximum logic low output found in device data sheet. Typically 0.4V.

$I_{SinkMax}$ = maximum sink current when the output transistor is on (logic low) found in device data sheet. Typically 3mA.

C_b = bus capacitance. Depends on width and length of PCB trace (see **Equation 164**), and the capacitance of the devices connected to the bus.

Example

Find a pull-up resistor for: V_{DD} = 5V, V_{OLMAX} = 0.4V, t_r = 300ns, and C_b = 100pF.

Answer

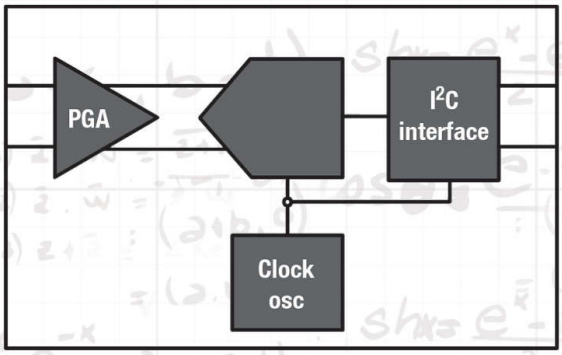
$$R_{Pull(Min)} = \frac{(V_{DD} - V_{OLMAX})}{I_{SinkMax}} = \frac{(5V - 0.4V)}{0.003A} = 1.53k\Omega$$
$$R_{Pull(Max)} = \frac{t_r}{(0.8473 \times C_b)} = \frac{300ns}{0.8473 \times 100pF} = 3.54k\Omega \quad (195)$$

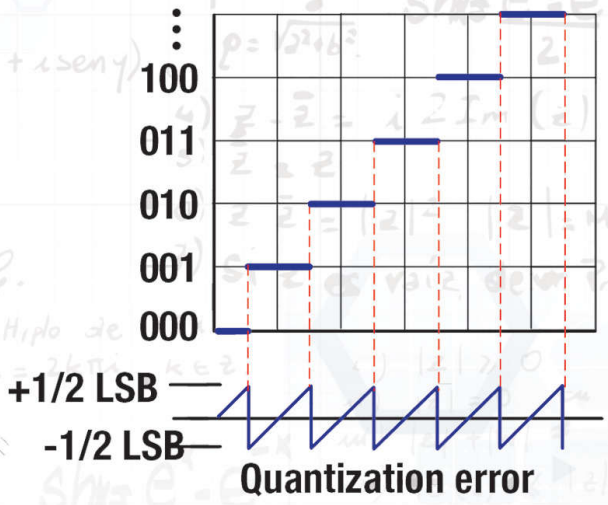
R_{Pull} = 2kΩ Selected as a standard value between $R_{Pull(Min)}$ and $R_{Pull(Max)}$

Notes

ADC

- ADC transfer function
- Quantization error of ADC
- Signal-to-noise ratio (SNR) from quantization noise only
- Total harmonic distortion (V_{RMS})
- Total harmonic distortion (dBc)
- AC signals
- DC signals
- Settling time and conversion accuracy
- ADC system noise calculation
- Effect of clock jitter on ADC SNR
- Notes





ADC transfer function

ADC definitions

Resolution = n	The number of bits used to quantify the input
Number of codes = 2^n	The number of output code combinations
Full-scale range input = FSR	Sets the converter input range and the LSB voltage
LSB = FSR / 2^n	The voltage step size of each LSB
Full-scale input voltage = (2^n – 1) • 1LSB	Full-scale input voltage of the ADC
Full-scale output code = 2^n – 1	Largest code that can be read
Transfer function: Output Code = round [V_{IN} / (FSR/2^n)]	Relationship between input voltage and output code

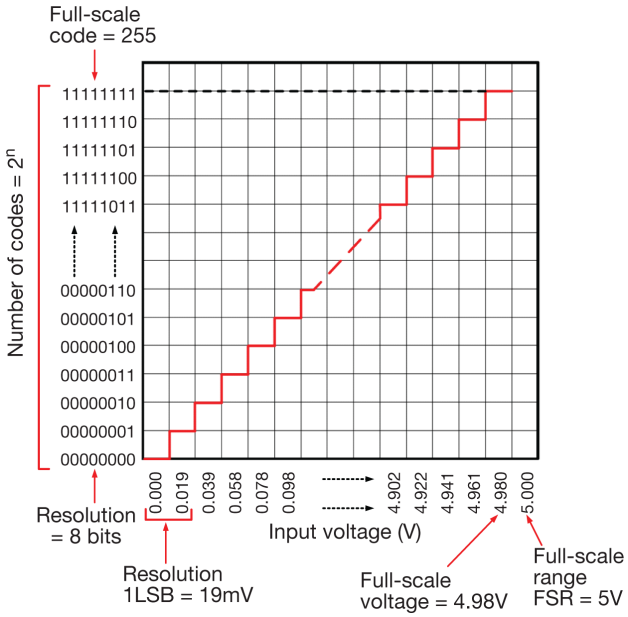


Figure 88. *ADC transfer function*

ADC resolution for unipolar

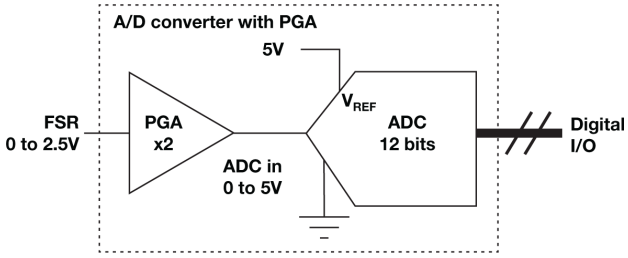


Figure 89. *ADC full-scale range (FSR) unipolar*

Full-scale range (FSR) unipolar

Full-scale range

$$FSR = \frac{V_{REF}}{PGA} \quad (196)$$

One least significant bit

$$1\text{LSB} = \frac{\text{FSR}}{2^{\text{n}}} \tag{197}$$

Where

FSR = full-scale range

PGA = PGA gain

1LSB = one least significant bit or resolution of the data converter

n = resolution number of bits

V_{REF} = reference voltage

Example calculation for the circuit above

$$\text{FSR} = \frac{\text{V}_{\text{REF}}}{\text{PGA}} = \frac{5\text{V}}{2} = 2.5\text{V}$$
$$1\text{LSB} = \frac{\text{FSR}}{2^{\text{n}}} = \frac{2.5\text{V}}{2^{12}} = 610.35\mu\text{V} \tag{198}$$

ADC resolution for bipolar

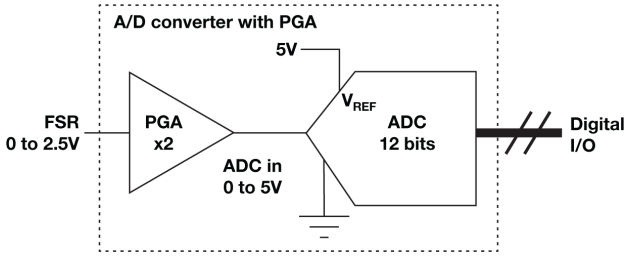


Figure 90. *ADC full-scale range (FSR) bipolar*

Full-scale range (FSR) bipolar

Full-scale range

$$\text{FSR} = \frac{\text{V}_{\text{REF}}}{\text{PGA}} \tag{199}$$

One least significant bit

$$1\text{LSB} = \frac{\text{FSR}}{2^{\text{n}}} \tag{200}$$

Where

FSR = full-scale range

PGA = PGA gain

1LSB = one least significant bit or resolution of the data converter

n = resolution number of bits

V_{REF} = reference voltage

Example calculation for the circuit above

$$\mathrm{FSR} = \frac{\pm \mathrm{V_{REF}}}{\mathrm{PGA}} = \frac{\pm 2.5\mathrm{V}}{2} = \pm\, 1.25\mathrm{V} \Rightarrow 2.5\mathrm{V}$$
$$1\mathrm{LSB} = \frac{\mathrm{FSR}}{2^{\mathrm{n}}} = \frac{2.5\mathrm{V}}{2^{12}} = 610.35\mu\mathrm{V} \quad (201)$$

Resolution voltage vs. full-scale range

Table 35. LSB voltage vs. resolution and reference voltage

		FSR (Full-Scale Range)			
		1.024V	1.25V	2.048V	2.5V
Resolution	8	4 mV	4.88 mV	8 mV	9.76 mV
	10	1 mV	1.22 mV	2 mV	2.44 mV
	12	250 µV	305 µV	500 µV	610 µV
	14	52.5 µV	76.3 µV	125 µV	152.5 µV
	16	15.6 µV	19.1 µV	31.2 µV	38.14 µV
	18	3.91 µV	4.77 µV	7.81 µV	9.53 µV
	20	0.98 µV	1.19 µV	1.95 µV	2.384 µV
	22	244 nV	299 nV	488 nV	596 nV
	24	61 nV	74.5 nV	122 nV	149 nV

Table 36. LSB voltage vs. resolution and reference voltage

		FSR (Full-Scale Range)			
		3V	3.3V	4.096V	5V
Resolution	8	11.7 mV	12.9 mV	16 mV	19.5 mV
	10	2.93 mV	3.222 mV	4 mV	4.882 mV
	12	732 µV	806 µV	1 mV	1.221 mV
	14	183 µV	201 µV	250 µV	305 µV
	16	45.77 µV	50.35 µV	62.5 µV	76.29 µV
	18	11.44 µV	12.58 µV	15.6 µV	19.07 µV
	20	2.861 µV	3.147 µV	3.91 µV	4.768 µV
	22	715 nV	787 nV	976 nV	1.192 µV
	24	179 nV	196 nV	244 nV	298 nV

Quantization error of ADC

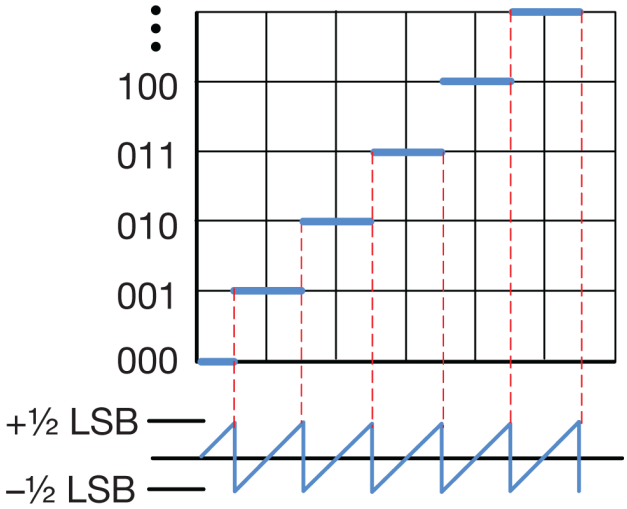


Figure 91. *Quantization error of an ADC converter*

Quantization error

The error introduced as a result of the quantization process. The amount of this error is a function of the resolution of the converter. The quantization error of an ADC converter is ½ LSB. The quantization error signal is the difference between the actual voltage applied and the ADC output (**Figure 91**). The RMS of the quantization signal is $1\text{LSB}/\sqrt{12}$.

Signal-to-noise ratio (SNR) from quantization noise only

$$\text{MaxRMSSignal} = \frac{\text{FSR}/2}{\sqrt{2}} = \frac{1\ \text{LSB} \times 2^{\text{N}-1}}{\sqrt{2}} \tag{202}$$

$$\text{RMSNoise} = \frac{1\ \text{LSB}}{\sqrt{12}} \text{from quantization only} \tag{203}$$

$$\text{SNR} = \frac{\text{MaxRMSSignal}}{\text{RMSNoise}} = \frac{1\ \text{LSB} \times 2^{\text{N}-1}/\sqrt{2}}{1\ \text{LSB}/\sqrt{12}} = 2^{\text{N}-1}\sqrt{6} \tag{204}$$

$$\text{SNR(dB)} = 20\log(\text{SNR}) = [20\log(2)]\text{N} + 20\log\left(\frac{\sqrt{6}}{2}\right) \tag{205}$$

$$\text{SNR(dB)} \approx 6.02\text{N} + 1.76 \tag{206}$$

Where

FSR = full-scale range of the ADC converter

1LSB = the voltage of 1LSB, $V_{REF}/2^n$

N = the resolution of the ADC converter

MaxRMSSignal = the RMS equivalent of the ADC's full-scale input

RMSNoise = the RMS noise from quantization

SNR = the ratio of RMS signal to RMS noise

Example

What is the SNR for an 8-bit ADC converter with 5V reference, assuming only quantization noise?

Answer

$SNR = 2^{N-1}\sqrt{6} = 2^{8-1}\sqrt{6} = 314$

$SNR(dB) = 20\log(314) = 49.9\ dB$

$SNR(dB) = 6.02(8) + 1.76 = 49.9\ dB$

Total harmonic distortion (V_{RMS})

$$\mathrm{THD}(\%) = \left(\frac{\mathrm{RMSDistortion}}{\mathrm{MaxRMSSignal}}\right) \cdot 100 = \frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + \ldots + V_n{}^2}}{V_1} \cdot 100 \quad (207)$$

$$\mathrm{THD(dB)} = 20\log\left(\frac{\mathrm{RMSDistortion}}{\mathrm{MaxRMSSignal}}\right) \quad (208)$$

Where

THD = Total Harmonic Distortion, the ratio of the RMS distortion to the RMS signal

RMSDistortion = the RMS sum of all harmonic components

MaxRMSSignal = the RMS value of the input signal

V_1 = the fundamental, generally the input signal

V_2, V_3, V_4, …V_n = harmonics of the fundamental

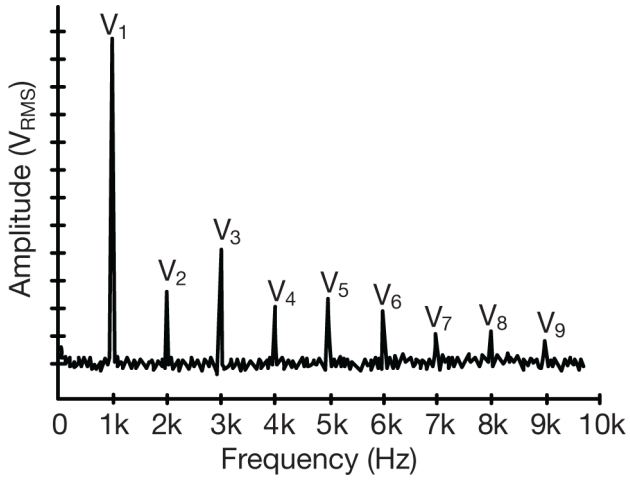


Figure 92. *Fundamental and harmonics in V_{RMS}*

Total harmonic distortion (dBc)

$$\mathrm{THD(dBc)} = 10\log\left[10^{\left(\frac{D_2}{10}\right)} + 10^{\left(\frac{D_3}{10}\right)} + 10^{\left(\frac{D_4}{10}\right)} + \ldots + 10^{\left(\frac{D_n}{10}\right)}\right] \quad (209)$$

Where

THD = Total Harmonic Distortion. The ratio of the RMS distortion to the RMS signal.

D_1 = the fundamental, generally the input signal. This is normalized to 0 dBc.

D_2, D_3, D_4, …D_n = harmonics of the fundamental measured relative to the fundamental

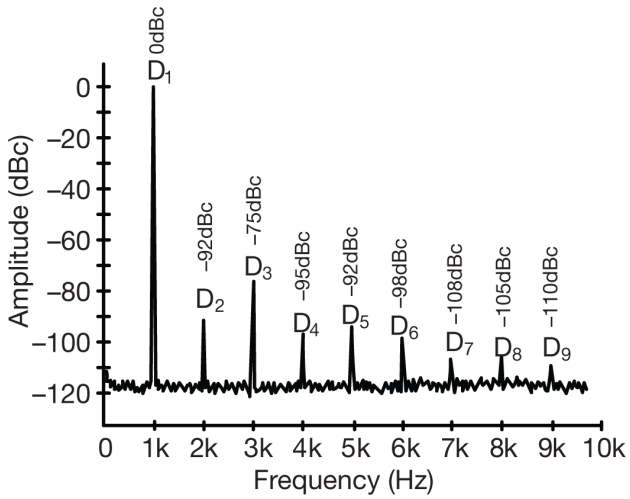


Figure 93. *Fundamental and harmonics in dBc*

Example

Determine THD for the example above.

Answer

$$\mathrm{THD(dBc)} = 10\log\left[10^{\left(\frac{-92}{10}\right)} + 10^{\left(\frac{-75}{10}\right)} + 10^{\left(\frac{-95}{10}\right)} + \ldots + 10^{\left(\frac{-110}{10}\right)}\right] \quad (210)$$

$$\mathrm{THD(dBc)} = -74.76\ \mathrm{dB}$$

AC signals

Signal-to-noise and distortion (SINAD) and effective number of bits (ENOB)

$$\mathrm{SINAD(dB)} = 20\log\left(\frac{\mathrm{MaxRMSSignal}}{\sqrt{\mathrm{RMSNoise}^2 + \mathrm{RMSDistortion}^2}}\right) \quad (211)$$

$$\mathrm{SINAD(dB)} = -20\log\left(\sqrt{10^{\left(\frac{-\mathrm{SNR(dB)}}{10}\right)} + 10^{\left(\frac{\mathrm{THD(dB)}}{10}\right)}}\right) \quad (212)$$

$$\text{ENOB} = \frac{\text{SINAD(dB)} - 1.76\text{dB}}{6.02} \tag{213}$$

Where

MaxRMSSignal = the RMS equivalent of the ADC's full-scale input

RMSNoise = the RMS noise integrated across the ADC converters

RMSDistortion = the RMS sum of all harmonic components

SINAD = the ratio of the full-scale signal-to-noise ratio and distortion

THD = Total Harmonic Distortion. The ratio of the RMS distortion to the RMS signal.

SNR = the ratio of RMS signal to RMS noise

Example

Calculate the SNR, THD, SINAD and ENOB given the following information:

MaxRMSSignal = 1.76 V_{RMS}

RMSDistortion = 50 μV_{RMS}

RMSNoise = 100 μV_{RMS}

Answer

$$\text{SNR(dB)} = 20\log\left(\frac{1.76\ \text{V}_{\text{RMS}}}{100\ \mu\text{V}_{\text{RMS}}}\right) = 84.9\ \text{dB}$$

$$\text{THD(dB)} = 20\log\left(\frac{50\ \mu\text{V}_{\text{RMS}}}{1.76\ \text{V}_{\text{RMS}}}\right) = -90.9\ \text{dB}$$

$$\text{SINAD(dB)} = 20\log\left(\frac{1.76\ \text{V}_{\text{RMS}}}{\sqrt{\left(100\ \mu\text{V}_{\text{RMS}}\right)^2 + \left(50\ \mu\text{V}_{\text{RMS}}\right)^2}}\right) = 83.9\ \text{dB} \tag{214}$$

$$\text{SINAD(dB)} = -20\log\left(\sqrt{10^{\left(\frac{-84.9\ \text{dB}}{10}\right)} + 10^{\left(\frac{-90.9\ \text{dB}}{10}\right)}}\right) = 83.9\ \text{dB}$$

$$\text{ENOB} = \frac{83.9\text{dB} - 1.76\text{dB}}{6.02} = 13.65$$

DC signals

Noise free resolution and effective resolution

$$\text{NoiseFreeResolution} = \log_2\left(\frac{2^{\text{N}}}{\text{PeaktoPeakNoiseinLSB}}\right) \tag{215}$$

$$\text{EffectiveResolution} = \log_2\left(\frac{2^{\text{N}}}{\text{rmsNoiseinLSB}}\right) \tag{216}$$

$$\text{PeaktoPeakNoiseinLSB} \approx 6.6 \times \text{rmsNoiseinLSB} \tag{217}$$

$$\text{EffectiveResolution} \approx \text{NoiseFreeResolution} + 2.7 \tag{218}$$

Note

The maximum effective resolution is never greater than the ADC resolution. For example, a 24-bit converter cannot have an effective resolution greater than 24 bits.

Example

What is the noise-free resolution and effective resolution for a 24-bit converter assuming the peak-to-peak noise is 7 LSBs?

Answer

$$\text{NoiseFreeResolution} = \log_2\left(\frac{2^{24}}{7}\right) = 21.2$$

$$\text{EffectiveResolution} = \log_2\left(\frac{2^{24}}{\frac{7}{6.6}}\right) = 23.9 \tag{219}$$

$$\text{EffectiveResolution} = 21.2 + 2.7 = 23.9$$

Settling time and conversion accuracy

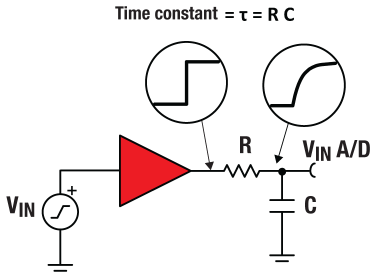


Figure 94. *Settling time for RC circuit-related to ADC converters*

Table 37. Conversion accuracy achieved after a specified time

Settling time in time constants (N_{TC})	Accuracy in bits (N)	Settling time in time constants (N_{TC})	Accuracy in bits
1	1.44	10	14.43
2	2.89	11	15.87
3	4.33	12	17.31
4	5.77	13	18.76
5	7.21	14	20.20
6	8.66	15	21.64
7	10.10	16	23.08
8	11.54	17	24.53
9	12.98	18	25.97

$$N = \log_2\left(e^{-N_{TC}}\right) \tag{220}$$

Where

N = the number of bits of accuracy the RC circuit has settled to after N_{TC} number of time constants

N_{TC} = the number of RC time constants. Where one time constant equals R·C.

Note

For a FSR step. For single-ended input ADC with no PGA front end, FSR (full-scale range) = V_{REF}.

Table 38. Time required to settle to a specified conversion accuracy

Accuracy in bits (N)	Settling time in time constants (N_{TC})	Accuracy in bits (N)	Settling time in time constants (N_{TC})
8	5.5	17	11.78
9	6.24	18	12.48
10	6.93	19	13.17
11	7.62	20	13.86
12	8.32	21	14.56
13	9.01	22	15.25
14	9.70	23	15.94
15	10.40	24	16.64
16	11.04	25	17.33

$$N_{TC} = \ln\left(2^N\right) \tag{221}$$

Where

N_{TC} = the number of time constants required to achieve N bits of settling. Where one time constant equals R·C.

N = the number of bits of accuracy

Note: For a FSR step. For single-ended input ADC with no PGA front end, FSR (full-scale rangee) = V_{REF}.

ADC system noise calculation

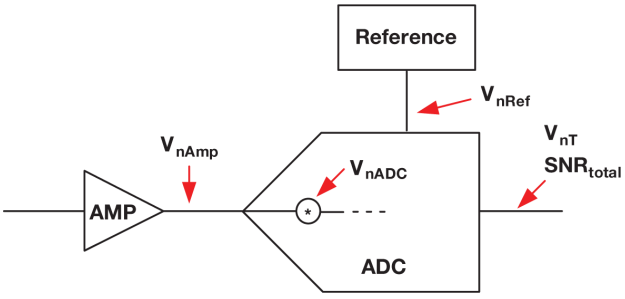


Figure 95. *ADC noise*

Full-scale RMS input

$$V_{FSR\_RMS} = \frac{V_{FSR} \cdot 0.707}{2} \quad (222)$$

Solve for noise

$$SNR_{ADC} = 20 \cdot \log\left(\frac{V_{FSR\_RMS}}{V_{nADC}}\right) \quad (223)$$

From ADC data sheet

$$V_{nADC} = \frac{V_{FSR\_RMS}}{10^{\left(\frac{SNR_{ADC}}{20}\right)}} \quad (224)$$

Total RMS noise

$$V_{nT} = \sqrt{(V_{nADC})^2 + (V_{nAmp})^2 + (V_{nRef})^2} \quad (225)$$

Where

V_{FSR} = the ADC full scale range from the data sheet

V_{FSR_RMS} = this finds the maximum RMS amplitude of a sine wave applied to an ADC. Dividing the ADC full scale range by 2 converts peak-to-peak to peak. Multiplying by 0.707 converts to RMS.

SNR_{ADC} = Data converter signal to noise ratio specification from data sheet

V_{nADC} = noise in volts RMS derived from the SNR equation. Converting noise to volts allows it to be combined with amplifier and reference noise.

V_{nAmp} = amplifier noise in volts RMS calculated or simulated using data sheet parameters

V_{nRef} = reference noise in volts RMS calculated or simulated using data sheet parameters

V_{nT} = total noise in volts RMS calculated by combining ADC, amplifier, and reference noise

Effect of clock jitter on ADC SNR

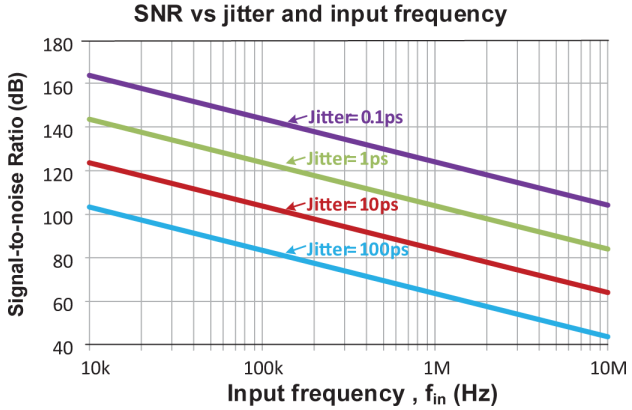


Figure 96. *SNR vs jitter and input frequency*

From ADC data sheet

$$\mathrm{SNR} = -20 \cdot \log\left(2 \cdot \pi \cdot f_{in} \cdot t_{jitter}\right) \quad (226)$$

SNR limitation from jitter including oversampling

$$\mathrm{SNR} = -20 \cdot \log\left(2 \cdot \pi \cdot f_{in} \cdot t_{jitter}\right) + 10 \cdot \log(\mathrm{OSR}) \quad (227)$$

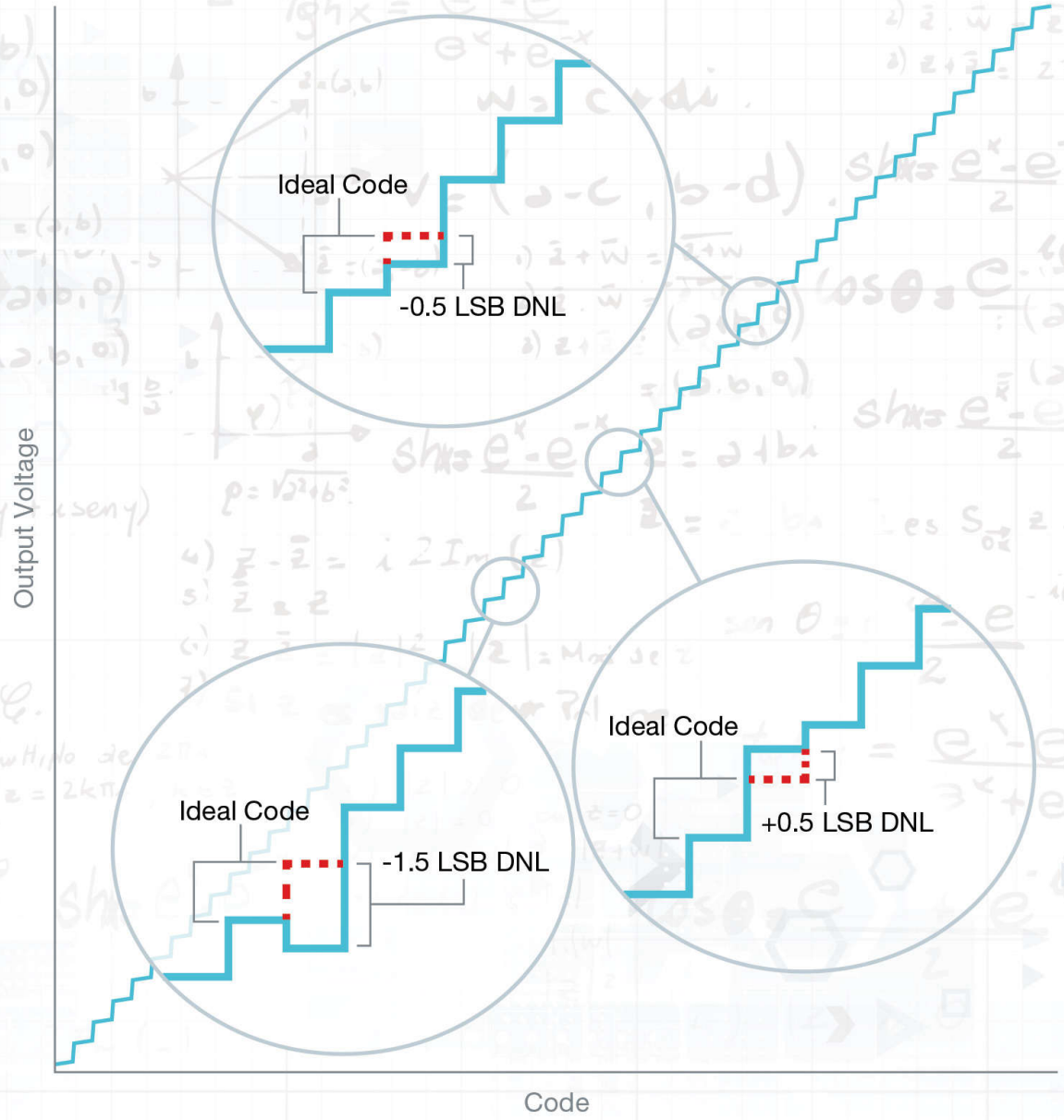
Where

f_{in}= input frequency (Hz)

t_{jitter} = ADC clock jitter time (seconds)

OSR = oversampling ratio

Notes



DAC errors

DAC definitions

Resolution = n	The number of bits used to quantify the output
Number of codes = 2^n	The number of input code combinations
Full-scale range output = FSR	Sets the converter output range and the LSB voltage
LSB = FSR / 2^n	The voltage step size of each LSB
Full-scale output voltage = (2^n – 1) × 1LSB	Full-scale output voltage of the DAC
Full-scale input code = 2^n – 1	Largest code that can be written
Transfer function: V_{OUT} = number of codes × (FSR/2^n)	Relationship between output voltage and input code

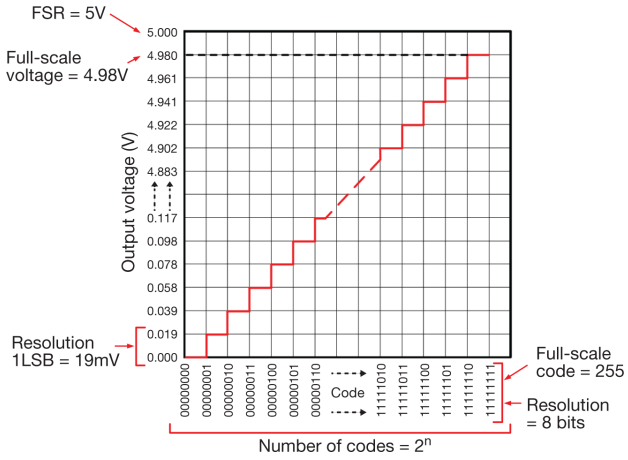


Figure 97. *DAC transfer function*

DAC offset error

Offset error is the y-axis intercept based on a two-point best fit measurement extrapolated to a zero input code. This is different from zero code error which is measured with Code = 0H and includes the nonlinear effects as the DAC output approaches zero volts.

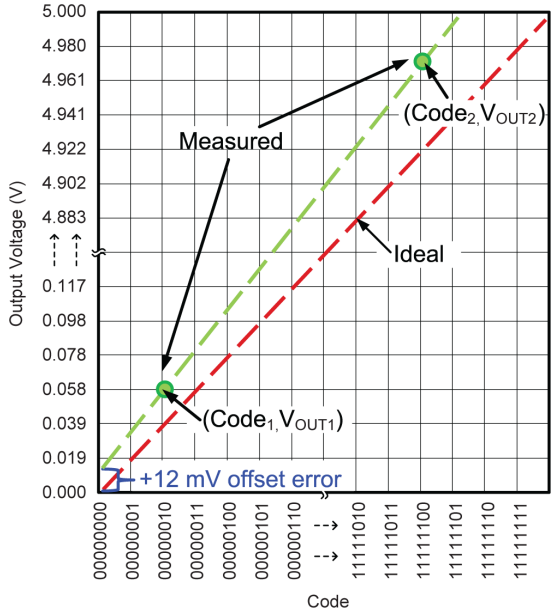


Figure 98. *Offset error illustration*

General equation for best fit line

$$V_{OUT} = m_m \cdot Code + Offset \quad (228)$$

Measured slope

$$m_m = \frac{V_{OUT2} - V_{OUT1}}{Code_2 - Code_1} \quad (229)$$

Offset

$$Offset = V_{OUT1} - m_m \cdot Code_1 \quad (230)$$

Where

V_{OUT} = DAC output voltage

m_m = measured slope

Code = input digital code

Offset = the offset of a best fit line

DAC gain error

Gain error describes the deviation from the ideal slope of the DAC transfer function. Similar to offset error, this specification is measured at the DAC output using a two- point line of best fit, which is then compared against the ideal gain and expressed in a percentage.

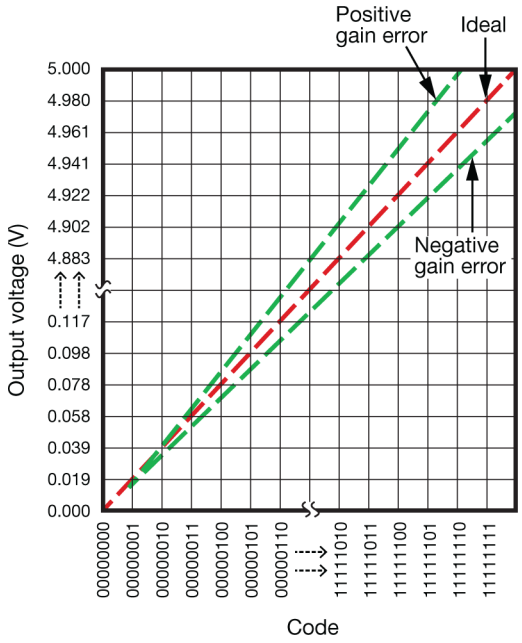


Figure 99. *Gain error illustration*

General equation for best fit line

$$V_{OUT} = m_m \cdot Code + Offset \quad (231)$$

Measured slope

$$m_m = \frac{V_{OUT2} - V_{OUT1}}{Code_2 - Code_1} \tag{232}$$

Gain error in percentage

$$GE = \left(\frac{m_m - m_{ideal}}{m_{ideal}}\right) \cdot 100 \tag{233}$$

Where

V_{OUT} = DAC output voltage

m_m = measured slope

Code = input digital code

Offset = the offset of a best fit line

Note

($Code_1$, V_{OUT1}) and ($Code_2$, V_{OUT2}) are two data points on the measured transfer function. See **Figure 98**.

DAC zero-code error / negative full-scale error

Zero-code error (sometimes called negative full-scale error) is an end-point error measured when all 0's are loaded into the DAC data register. For a DAC with bipolar outputs, this may also be called negative full-scale error. The intention is to describe how close to the negative rail the DAC output can get when set to the minimal output value. Zero-code error is different from offset error in that it includes the potentially nonlinear output swing limitations, whereas the offset error is the offset of the best fit transfer function. The specified test conditions will indicate what, if any, negative supply was used to help assess the swing to ground capability at zero code.

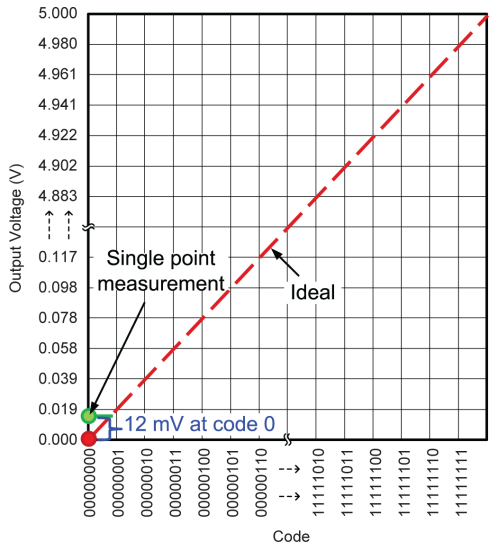


Figure 100. *Zero-code error illustration*

DAC bipolar zero error

Bipolar zero error is a special datasheet parameter reserved for DACs with bipolar voltage or current outputs. It describes the DAC error when set to mid-scale, assuming a symmetrical output span, where the ideal DAC should be 0V or 0A. This specification is the mid-scale combination of both offset and gain errors. The specification is arrived at based on statistical analysis and, therefore, mathematically the summation of offset and gain errors may not match this value exactly.

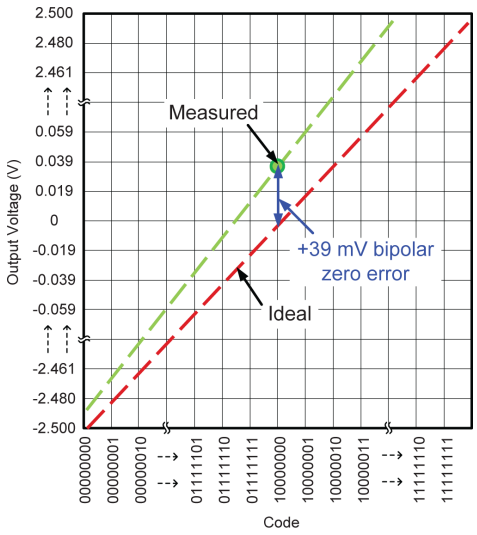


Figure 101. *Bipolar zero error illustration*

DAC full-scale error

Full-scale error is an end-point error measured when all 1's are loaded into the DAC data register. The intention is to describe how close to the positive rail the DAC output can get when set to the maximum output value. The specified test conditions will indicate what positive supply was used.

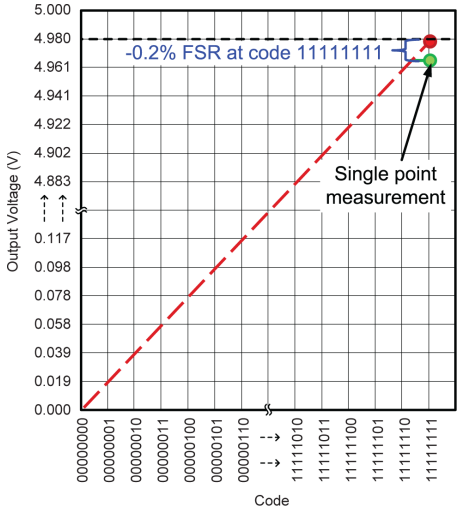


Figure 102. *Full-scale error illustration*

DAC non-linearity

DAC differential non-linearity

Differential non-linearity, or commonly abbreviated DNL, describes the actual measured step sizes versus ideal and is expressed in terms of least significant bits or LSBs. The electrical characteristics table of a DAC datasheet will only express a single minimum and maximum value, expressing the worst case observed across every code in the linear region of the DAC transfer function. When near the positive or negative rails, especially outside of the ranges defined by the high-code and low- code used to measure offset and gain errors, DNL performance will be degraded due to saturation near the rails. Most modern DACs are monotonic meaning that the output voltage will always increase as input codes increase. **Figure 103** shows both monotonic and non-monotonic DNL.

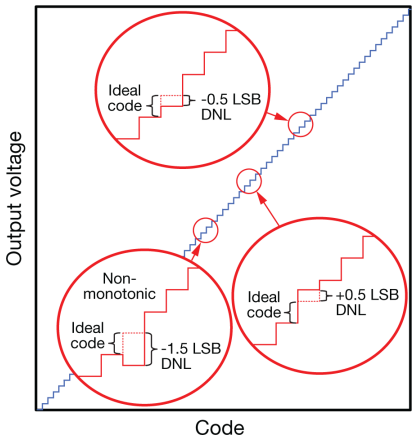


Figure 103. *DNL error illustration*

DAC integral non-linearity

INL (Integral Non-Linearity) is sometimes referred to as relative accuracy. This is the deviation of the transfer function from an end point fit. While DNL describes the relationship of actual code step-sizes to ideal, INL expresses the cumulative effects of sequential DNL errors. INL is the maximum deviation from an end point fit straight line. This error source cannot be corrected using a simple two point fit calibration.

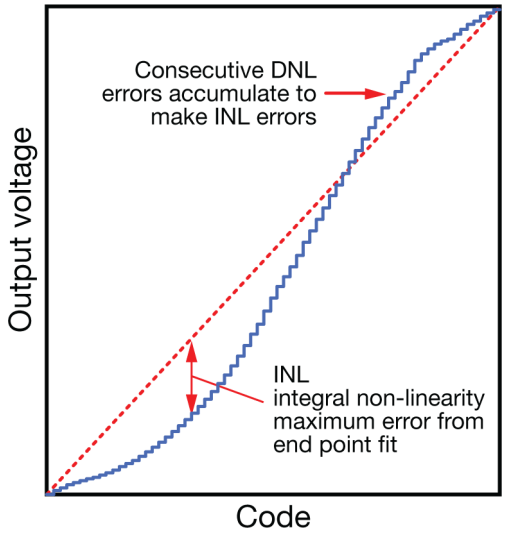


Figure 104. *INL error illustration*

DAC total unadjusted error

The equation below is for the total unadjusted error (or TUE). TUE is the statistical combinations of error sources in the linear region of operation for the DAC. In order to perform the above TUE calculation it is necessary to have each of the parametric error sources in the same units. **Table 7** shows the calculations required to convert to different units (e.g. from percentage to parts per million).

Gain error in percentage

$$\mathrm{TUE} = \sqrt{\mathrm{OffsetError}^2 + \mathrm{GainError}^2 + \mathrm{INLError}^2} \tag{234}$$

Where

OffsetError = the offset of a best fit line through the transfer function. See **Figure 98**.

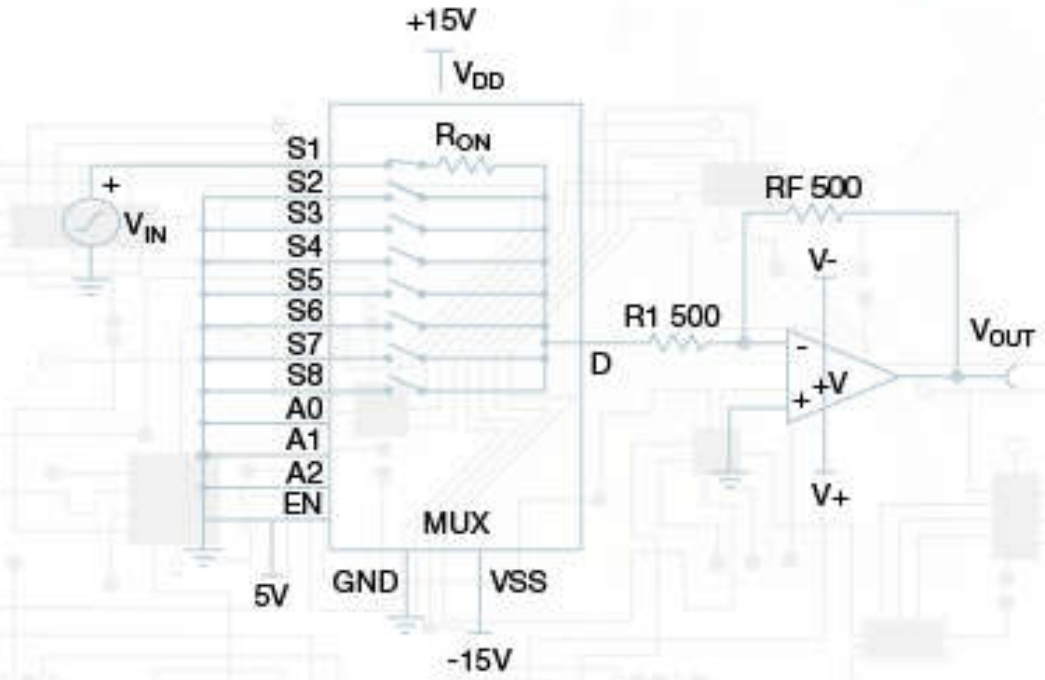
GainError = the difference between the ideal slope and the measured slope. See **Figure 99**.

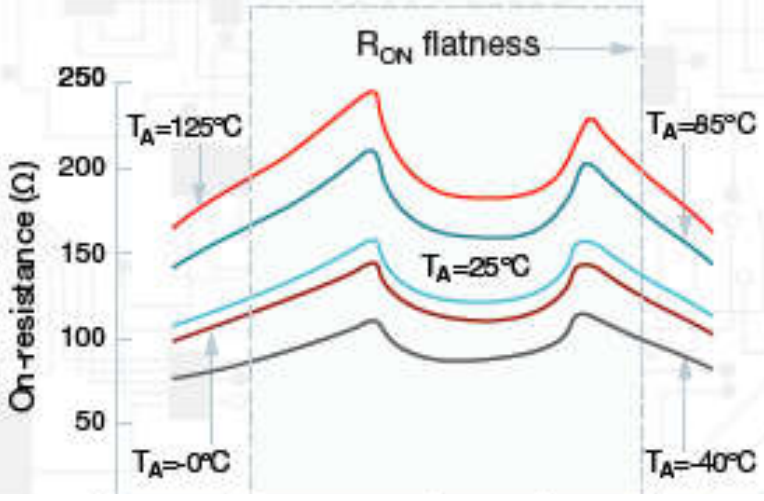
INLError = the maximum deviation from a best fit line through the transfer function. See **Figure 104**.

Notes

Multiplexer

- CMOS switch construction
- ON-resistance (R_{ON})
- R_{ON} flatness
- Effective op amp gain including MUX R_{ON}
- ON and OFF capacitance (C_{ON}/ C_{OFF})
- Leakage current
- Charge injection (Q_{INJ})
- Bandwidth (BW)
- Channel-to-channel crosstalk (X_{TALK})
- OFF-isolation
- Total harmonic distortion plus noise (THD+N)
- Notes





CMOS switch construction

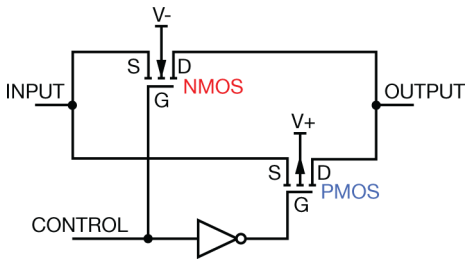


Figure 105. *Typical CMOS switch construction*

Typical CMOS switch elements

- Parallel combination of N channel and P channel FET
- Control signal that controls the state of the switch

ON-resistance (R_{ON})

Resistance between sources to drain terminal when switch is closed

- PMOS conducts for positive input voltages
- NMOS conducts for negative input voltages
- Combined RON is lower than individual resistance of the NMOS or PMOS that form the switch

Varies with

- MUX input voltage
- Operating ambient temperature

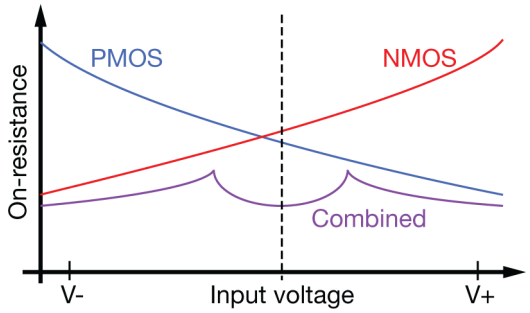


Figure 106. *Typical MUX ON-resistance curve vs input voltage*

R_{ON} flatness

Difference between maximum and minimum ON-resistance over a specified input range

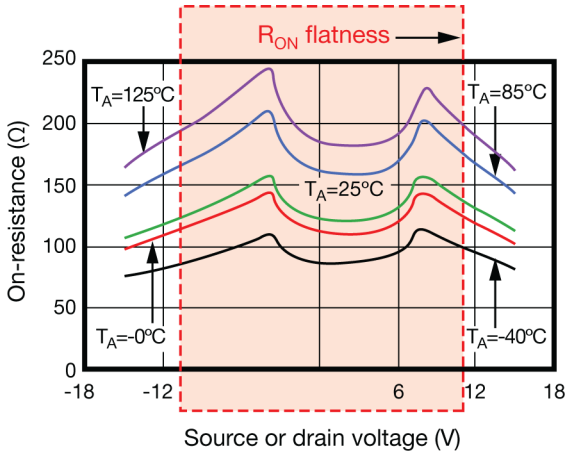


Figure 107. *R_{ON} flatness illustration*

Effective op amp gain including MUX R_{ON}

This section shows the impact of R_{ON} flatness on gain error and non-linearity. **Figure 107** shows the circuit and **Figure 108** shows the measured results.

Effective gain for op amp with MUX

$$AG = \frac{V_{OUT}}{V_{IN}} = \frac{-RF}{(R1 + R_{ON})} \tag{235}$$

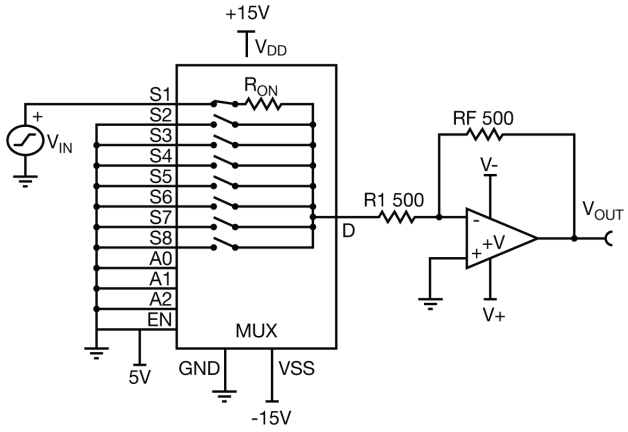


Figure 108. *Front-end MUX followed by an inverting amplifier stage*

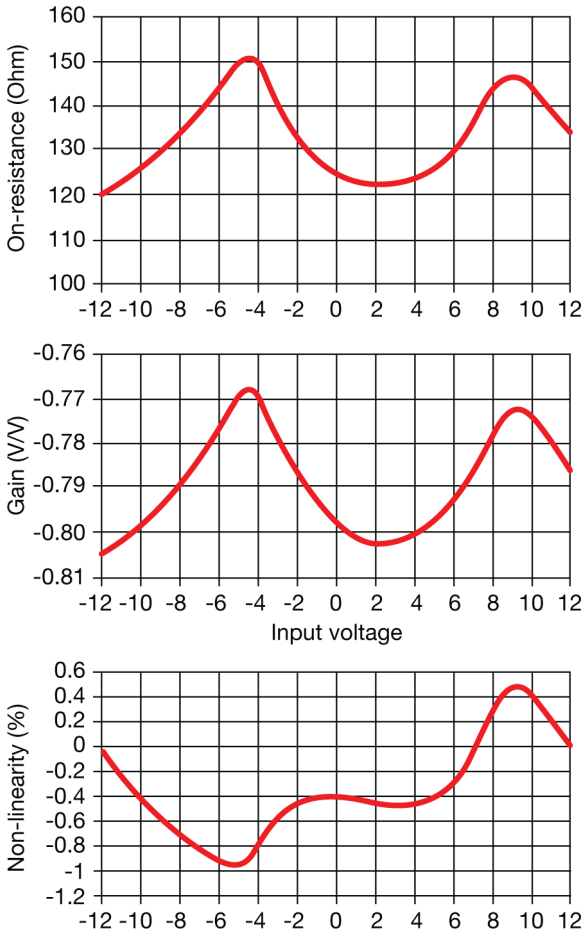


Figure 109. *Effect of varying R_{ON} causing gain error and non-linearity*

Design tips

- Use high impedance stage between MUX output and signal conditioning
- Use a multiplexer with lower R_{ON} (at the expense of other design trade-offs)

ON and OFF capacitance (C_{ON}/ C_{OFF})

- C_{OFF} = parasitic capacitance when the switch is OFF

$$C_{OFF} = C_S(\text{on source side}) \text{ or } C_D(\text{on drain side}) \quad (236)$$

- C_{ON} = parasitic capacitance when the switch is ON $C_{ON} \approx C_S + C_D$

$$C_{ON} \approx C_S + C_D \quad (237)$$

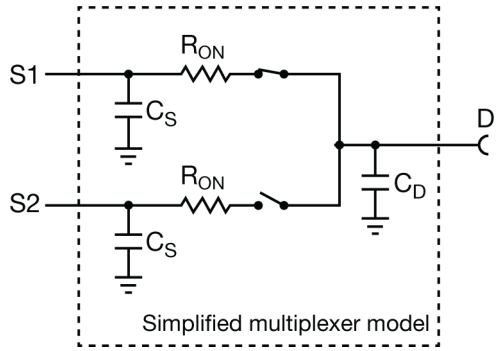


Figure 110. *Simplified model for MUX parasitic capacitance calculation*

Design tips

$$\text{Settling time} = t_{TRANSITION} + (R_{ON} \cdot C_D \cdot K) \tag{238}$$

Where

$t_{TRANSITION}$ = MUX channel-to-channel transition time (refer to MUX specification)

R_{ON} = switch ON-resistance between sources and drain

C_D = switch drain parasitic capacitance

K = number of time constants to settle to a N bit resolution ADC, K = ln(2^N)

MUX settling time with C_{LOAD} and R_{LOAD}

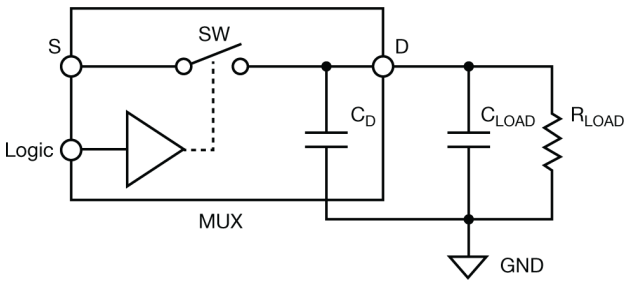


Figure 111. *Simplified model for MUX settling time calculation*

$$\text{Settling time} = t_{TRANSITION} + \frac{R_{ON} \cdot R_{LOAD}}{R_{ON} + R_{LOAD}}(C_{LOAD} + C_D) \cdot K \tag{239}$$

Where

$t_{TRANSITION}$ = MUX channel-to-channel transition time (refer to MUX specification)

R_{ON} = switch ON-resistance between sources and drain

R_{LOAD} = resistor connected to MUX output

C_{LOAD} = capacitor connected to MUX output

C_D = switch drain parasitic capacitance

K = number of time constants to settle to a N bit resolution ADC, K = ln(2^N)

Example

Determine the settling time of a MUX to 14-bit accuracy.

R_{ON}=125Ω; $C_{D(OFF)}$ =7.5pF

R_{LOAD}=1kΩ; C_{LOAD}=5pF

$t_{TRANSITION}$=92ns

Answer

$$\text{Settling time} = 92\text{ns} + \frac{125 \cdot 1000}{125 + 1000} \cdot (5\text{pF} + 7.5\text{pF}) \cdot \ln\left(2^{14}\right) = 105.5\text{ns} \quad (240)$$

Leakage current

Off leakage current

- $I_{S(OFF)}$= input leakage current flows through R_{SOURCE}
- $I_{D(OFF)}$ = output leakage current flows through R_L

$$V_{ERROR(OUTPUT)} = R_L \cdot I_{D(OFF)} \quad (241)$$

On leakage current

- $I_{D(ON)}$ = $I_{LEAKAGE}$

$$V_{ERROR(OUTPUT)} = (R_{ON} + R_{SOURCE}) \cdot I_{D(ON)} \quad (242)$$

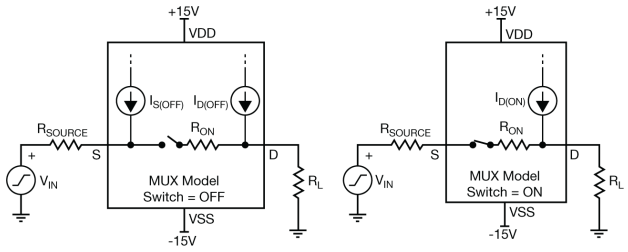


Figure 112. *Simplified models for OFF and ON leakage current through a MUX*

Example

Determine the Switch = ON error caused by MUX leakage current in an 18-bits system:

Assume R_L is a very high input impedance (R_L > 100MΩ, i.e. an op amp input)

R_{SOURCE} = 1MΩ

R_{ON} = 100Ω

$I_{D(ON)}$ = 100pA

V_{REF} = 5V

Answer

$$V_{LSB} = \frac{5V}{2^{18}} = 19.073\mu V$$

$$V_{ERROR} = I_{D(ON)} \cdot (R_{SOURCE} + R_{ON}) = (100pA) \cdot (1M\Omega + 100\Omega) = 100\mu V \quad (243)$$

$$BIT_{ERROR} = \frac{V_{ERROR}}{V_{LSB}} = \frac{100\mu V}{19.073\mu V} = 5.24 \text{ codes}$$

Charge injection (Q_{INJ})

Voltage change introduced at the output of switch when switch is turned ON or OFF

$$Q_{INJ} = (C_D + C_L) \cdot \Delta V_{OUT} \quad (244)$$

With large load capacitance, effect of C_D can be ignored

$$V_{ERROR} = \Delta V_{OUT} \approx \frac{Q_{INJ}}{C_L} \quad (245)$$

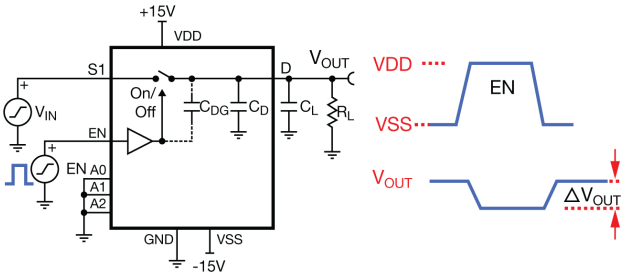


Figure 113. *Simplified model for MUX charge injection error*

A typical multiplexer charge injection curve vs. input (source) voltage is shown below.

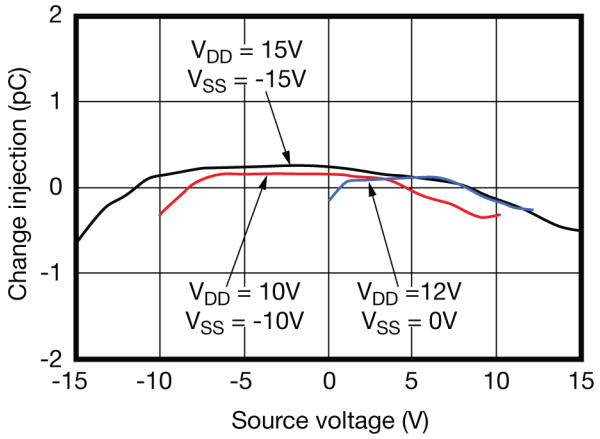


Figure 114. *Typical charge injection curve vs. source voltage*

Bandwidth (BW)

The frequency at which the output is attenuated by 3 dB from the pass band (DC) response.

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{R_L}{R_L + R_{ON}}\right) \cdot \left(\frac{1}{\frac{f}{f_{-3dB}} + 1}\right) \quad (246)$$

$$f_{-3dB} = \frac{1}{2\pi\left(\frac{R_L R_{ON}}{R_L + R_{ON}}\right)(C_D + C_L)} \quad (247)$$

If $R_L >> R_{ON}$:

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot R_{ON} \cdot (C_D + C_L)} \quad (248)$$

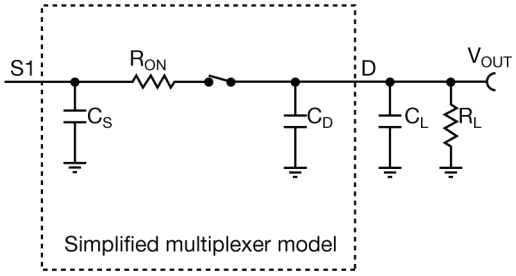


Figure 115. *Simplified model for MUX bandwidth calculation*

A typical multiplexer bandwidth response vs. frequency is shown below. The device exhibits a -3dB bandwidth of approximately 2GHz.

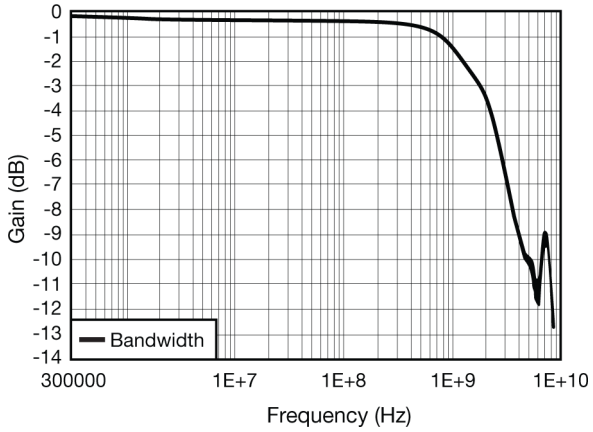


Figure 116. *Typical bandwidth response vs. frequency curve*

Channel-to-channel crosstalk (X_{TALK})

Crosstalk is defined as the amount of signal read at the input of an OFF channel (V_{OUT}), when V_S is applied to an ON channel.

$$X_{TALK} = 20 \cdot \log\left(\frac{V_{OUT}}{V_S}\right) \quad (249)$$

Where

V_{OUT} = voltage measured at source pin of OFF channel

V_S = voltage applied to source pin of ON channel

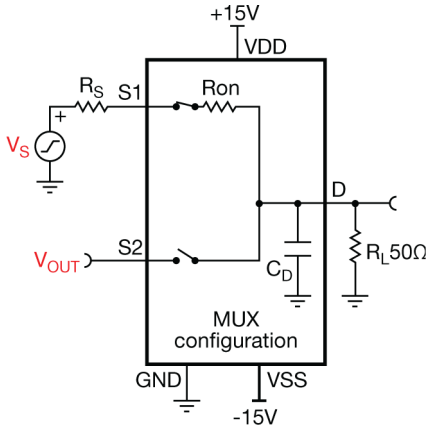


Figure 117. *Simplified model for MUX crosstalk calculation*

A typical multiplexer crosstalk vs. frequency is shown below for both adjacent and non-adjacent channels.

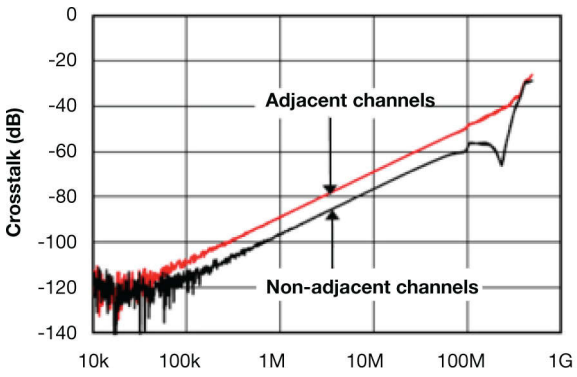


Figure 118. *Typical channel-to-channel crosstalk vs. frequency curve*

OFF-isolation

Voltage at output pin of a multiplexer when a known signal is applied at the source pin of an off-channel

$$\text{OFF\_isolation} = 20 \cdot \log\left(\frac{V_{OUT}}{V_{IN}}\right) \tag{250}$$

Where

V_{OUT} = voltage measured at source pin of OFF channel

V_{IN} = voltage applied at source pin of OFF channel

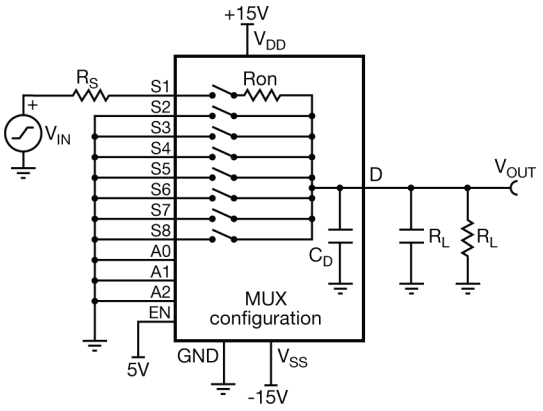


Figure 119. *Simplified model for MUX OFF-isolation calculation*

A typical multiplexer OFF-isolation vs. frequency is shown below for both adjacent and non-adjacent channels.

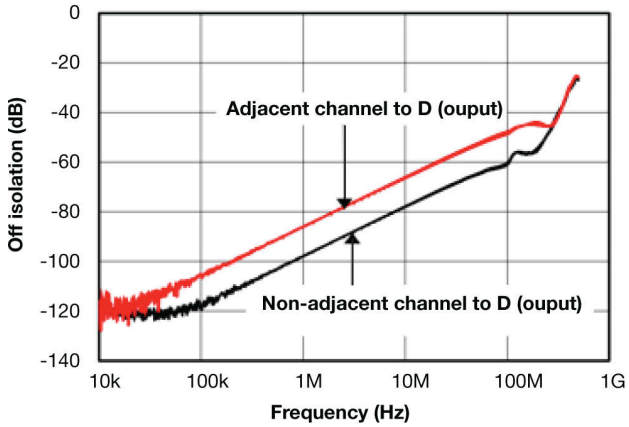


Figure 120. *Typical OFF-isolation vs. frequency curve*

Total harmonic distortion plus noise (THD+N)

- The ratio of the sum of all harmonic components and total RMS noise to the fundamental signal at the multiplexer output
- Highly dependent on the ON-resistance (R_{ON}) of the multiplexer

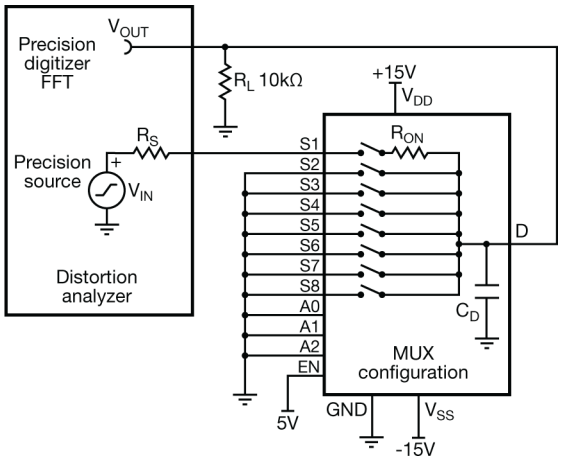


Figure 121. *Typical THD+ measurement setup*

A typical multiplexer THD+N vs. frequency curve is shown below

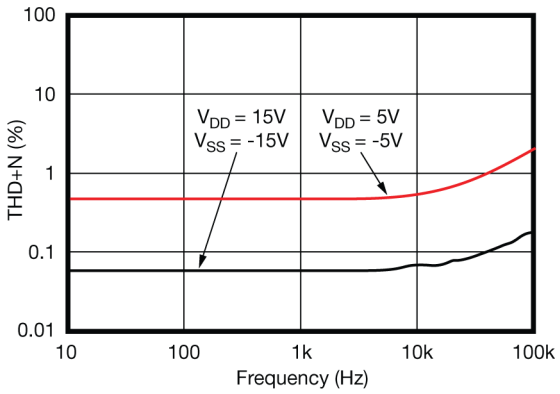


Figure 122. *Typical THD+N vs. frequency curve*

Design tips

- Use high impedance stage between MUX output and signal conditioning
- Use a multiplexer with lower R_{ON} (at the expense of other design trade-offs)

Notes

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